Technology Brief

Western Digital and the 3D NAND Revolution

Understanding 3D NAND Technology and Its Future Challenges

Avi Klein
Scott Harlin

Published October, 2017

Western Digital®

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For lower process nodes, planar NAND is no longer viable.

Introduction

For decades, two-dimensional planar NAND flash memory has reduced solid-state storage cost while improving performance and capacity. Beginning with 160 nanometer (nm) lithography in 2001, to 15nm in 2015, but for lower process nodes, planar NAND is no longer viable.

With the technology node shrink, the distances between the adjacent cells, as well as the dimension of the cells themselves, are decreasing. As cell-to-cell spacing decreases, it becomes more difficult to fit the insulating layers in this space, and consequently, the proximity effect increases, resulting in processing and reliability challenges. Figure 1 depicts the NAND flash memory evolution.

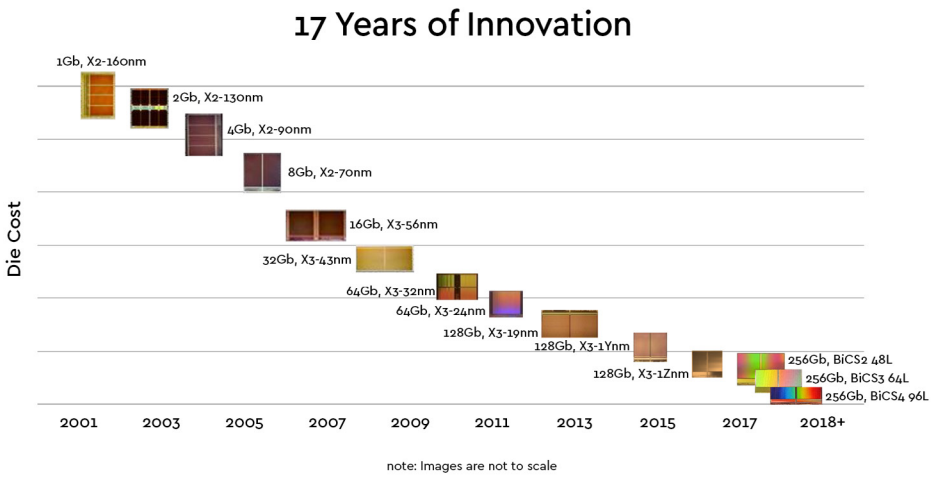

Figure 1: NAND Flash Memory Evolution

Another limitation is caused by patterning. During the photolithography process, light is used to transfer a geometric pattern from a mask to a photoresist on the chip to create electrical circuits. Currently, the lithographic technology is unable to generate a light wavelength that can draw the finer geometries needed. It is for this reason that repeated patterning steps are necessary, which in turn, increases costs. In addition, there are not enough electrons to reliably distinguish between bit 0 and 1 for sub-15nm shrinks. These limitations are described in Figure 2.

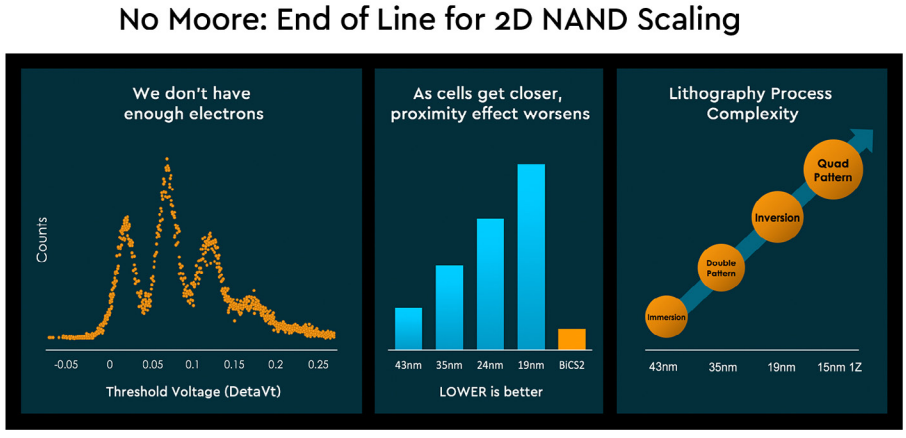

Figure 2: Limitations of 2D NAND

To overcome the limitations of 2D planar NAND technology, the industry has introduced 3D NAND which provides higher performance, better reliability, and lower power consumption when compared to 2D

To overcome the limitations of 2D planar NAND technology, the industry has introduced 3D NAND which provides higher performance, better reliability and lower power consumption when compared to 2D. Furthermore, 3D NAND is able to boost existing and future applications, and is designed to reduce costs by choosing the optimal number of layers.

3D NAND Overview

In contrast to traditional 2D planar NAND designs, 3D NAND has a vertical structure with layered cells in three-dimensional stacks. This vertical NAND string structure achieves high density without the need to shrink the cell lithography common with 2D NAND. The new flash technology is called BiCS (Bit Cost Scalable) with a schematic shown in Figure 3.

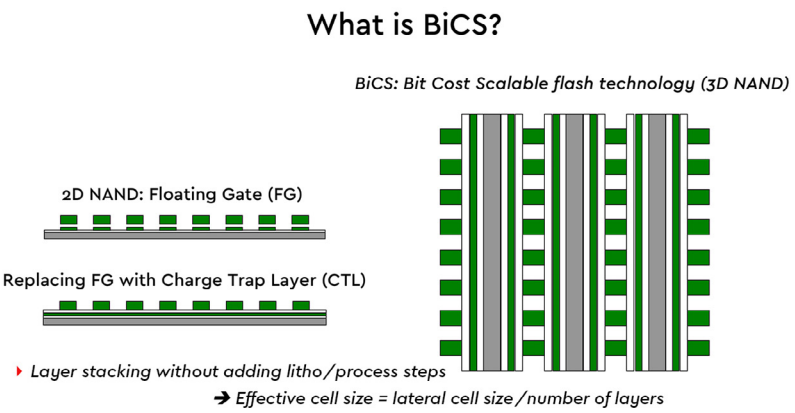

Figure 3: Description of BiCS 3D NAND

If we compare 3D NAND to 2D NAND, it's similar to building skyscrapers in the city instead of two-story houses in suburbia as outlined in Figure 4.

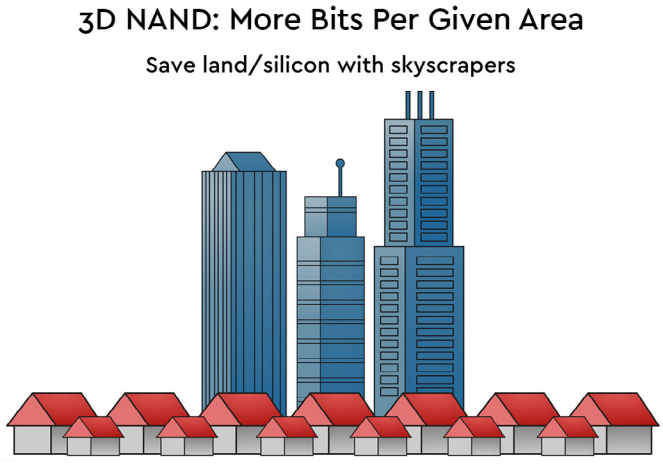

Figure 4: 2D NAND to 3D NAND Real Estate Analogy

3D NAND algorithms are simpler, enabling faster and more efficient performance.

3D NAND (BiCS) Technology

Western Digital's 3D NAND (BiCS) technology is able to break the 2D scaling ceiling by using the vertical dimension to stack more cells per unit area, while at the same time, relaxing the X-Y dimension of the basic cell. Scaling is achieved by adding more layers of cells on top of each other, like floors of a skyscraper. The X-Y relaxation reduces the proximity effect (i.e. cell-to-cell interference), which makes writing of data significantly faster while reducing power consumption.

In general, NAND flash programming speed is affected by the complexity of the program algorithms that write the data. 2D planar NAND flash requires very precise sets of complex program algorithms to prevent errors induced by cell-to-cell interference. These complex algorithms require additional time for data to be written, resulting in slower speed. The 3D NAND algorithms are simpler, enabling faster and more efficient performance.

When the process technology scales, the 2D NAND proximity effect increases due to a narrow floating gate to floating gate (FG-FG) space. However, in 3D NAND, each memory cell can reduce the proximity effect because of Bit Line (BL) shielding. Figure 5 shows the proximity effect in BiCS with respective contributions of Bit Line and Word Line descriptions to the overall effect:

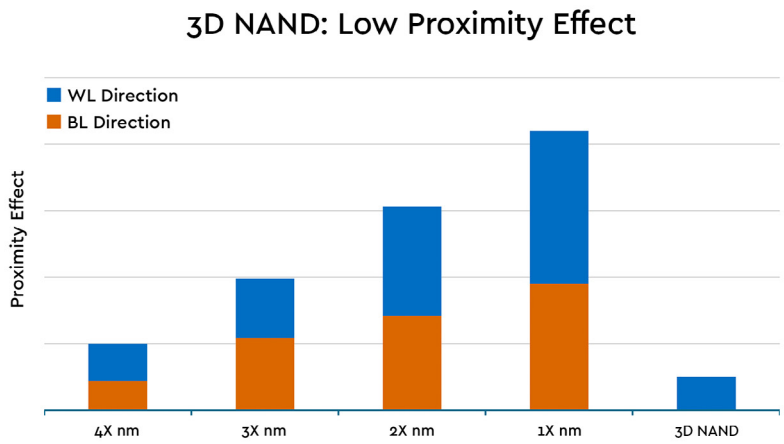

Figure 5: Proximity Effect in 3D NAND

There are several features in Western Digital's 3D NAND technology that differentiate it from others. First of all, Charge Trap Layer (CTL) technology is used instead of Floating Gate (FG) which simplifies the architecture as well as the manufacturing process, and improves reliability. The non-conductive CTL acts as an insulator, reducing the number of errors while increasing reliability margins, overcoming the drawbacks associated with the conductive floating gate technology used in 2D NAND. Figure 6 shows a cross-section of a 3D NAND memory cell.

3D NAND has a higher number of electrons per state when compared to 2D NAND (with similar bit density), and therefore, reduces errors and provides better reliability margins.

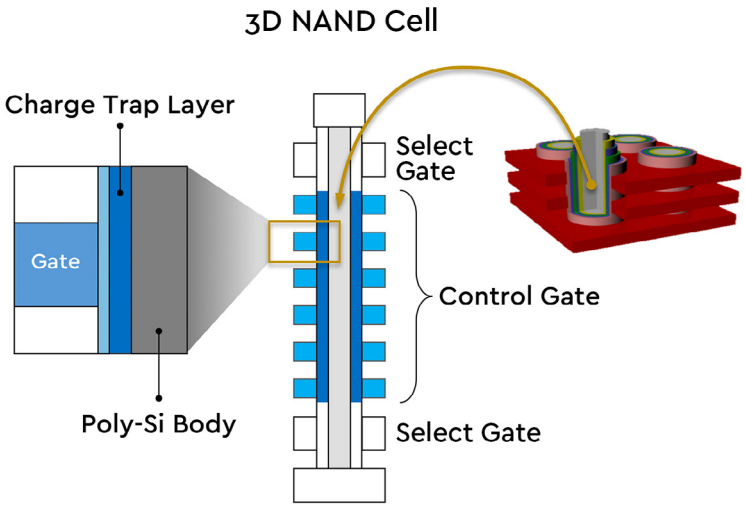

Figure 6: Cross-section of a 3D NAND Memory Cell

Secondly, the memory cell layers are connected by vertical NAND strings that run through a cylindrical channel. The memory cell's cylindrical shape also enables more charge per state. As a result, 3D NAND has a significantly higher number of electrons per state when compared to 2D NAND with similar bit density, and therefore, reduces errors and provides better reliability margins.

The memory cell is a metal-oxide nitride-oxide semiconductor (MONOS) structure with a continuous CTL along the memory hole as shown in Figure 7.

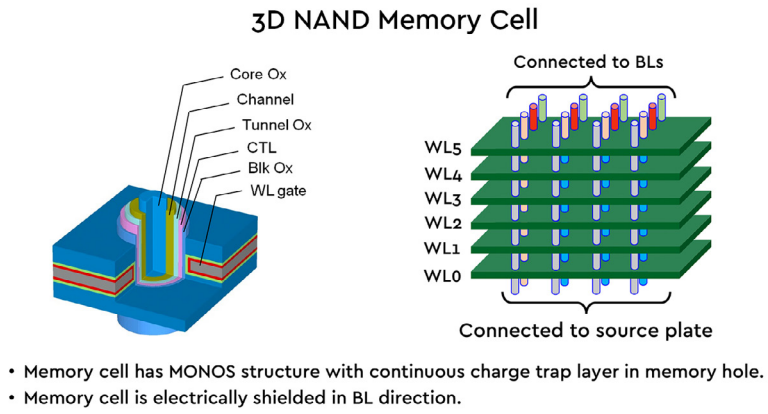

Figure 7: 3D NAND Memory Cell

The effective memory cell size can be larger than the latest 2D NAND offerings without area penalty due to more relaxed dimensions of 3D NAND's circular cell. As a result, the larger cell size can reduce sensitivity to electron loss and noise. Figure 8 shows a comparison of the cell dimensions of 2D NAND (left) vs 3D NAND (right).

Its optimized circular cell design improves performance as well as the number of Program/Erase cycles, which in turn, improves endurance and allows for more Terabytes written over a longer period of time.

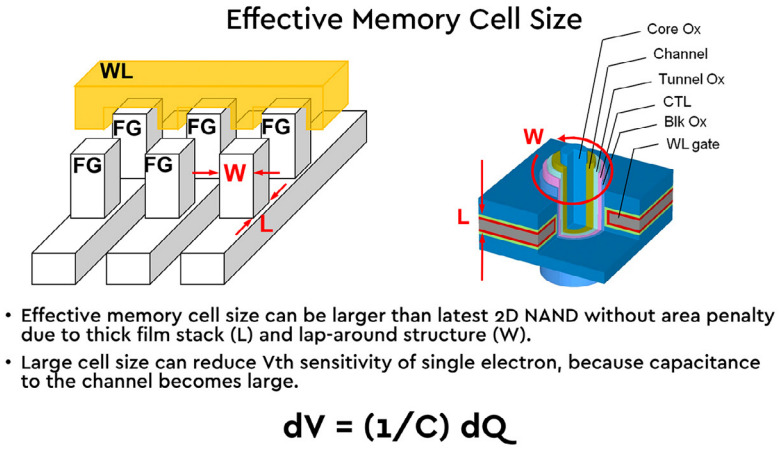

Figure 8: Effective Memory Cell Size

The combination of the CTL, along with relaxed design rules in the X-Y dimension (enabling larger cell critical dimensions), allow for more electrons to be stored in the larger 3D NAND cell. Its optimized circular cell design improves performance as well as the number of Program/Erase cycles, which in turn, improves endurance and allows for more Terabytes Written (TBW) over a longer period of time.

3D NAND Architecture

There are many similarities between 2D NAND and 3D NAND that make it a straightforward extension of NAND scaling. For example, the typical functions of Write, Erase and Read rely on the same physical mechanisms as 2D NAND, minus a few internal adjustments attributed to the use of a CTL. Also, the addressing scheme is similar in the way that Word Lines and Bit Lines are used. The trend of stacking more and more layers of Word Lines vertically, and the organization of the memory array, can form very large blocks and therefore sophisticated solutions are needed to overcome this large block issue.

Figure 9 depicts the 3D NAND architecture. The main architectural differences is that the NAND string (channel) is now vertical, and therefore the Word Lines are organized in layers on top of each other. There are additional changes in the architecture that are needed to optimize interconnections between the layers and to achieve optimal die density.

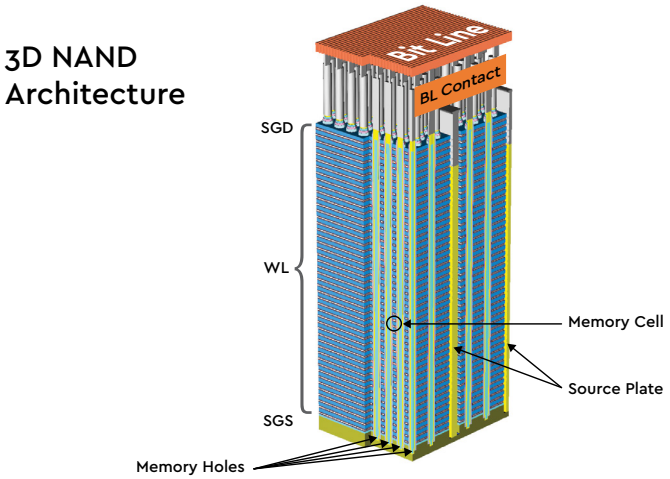

Figure 9: 3D NAND Architecture

Complexity has moved to etch and deposition processing – especially as holes become deeper when layers are added.

In 2017, Western Digital announced sampling of the industry's densest 3D NAND flash memory chips which can stack 96 layers on top of one another, deliver up to 1Tb of storage capacity. Together with its technology partner Toshiba, Western Digital also announced plans to produce 64 layer 3D NAND with four bits per cell and an industry leading storage capacity of 768Gb, enabling even larger storage densities in a smaller physical footprint.

3D NAND Challenges

Achieving high density at lower cost does not come for free and there are several challenges in the realization of the 3D NAND potential. From a manufacturing perspective, lithography has become less critical as the complexity has moved to etch and deposition processing – especially as holes become deeper when layers are added. Figure 10 shows the evolution of BiCS scalability. Since BiCS5 has additional layers when compared to BiCS4, the complexity also increases.

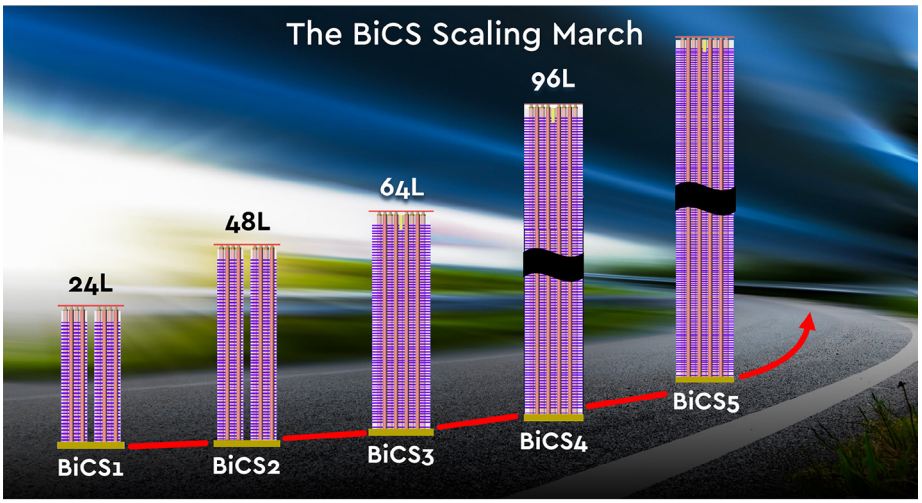

Figure 10: The BiCS Scaling March

Architectural solutions are developed to accommodate the complexity of very large blocks. Defect management and yield learning rates are other challenges that require sophisticated techniques to shorten time-to-market. Last, but certainly not the least, new use cases and applications require an ever-growing need for power, performance and reliability.

Western Digital is well positioned to address these challenges based on decades of continuous leadership in data storage.

3D NAND Availability

3D NAND will be embedded within servers, flash arrays, storage devices, connected automobiles and factories, as well as many other storage platforms, because it addresses the challenges associated with 2D planar NAND scaling. It achieves much higher capacities in the same physical footprint at a lower cost per bit, while providing better performance and higher reliability to address the future deluge of data.

USB flash drives, microSD cards, and client SSDs are some of the first products to widely adopt 3D NAND technology.

Flash solutions built on BiCS2 and BiCS3 3D NAND technologies are already being shipped to customers. USB flash drives, microSD cards, and client SSDs are some of the first products to widely adopt 3D NAND technology.

USB Flash Drives:

Provides removable and rewritable flash memory storage that plugs directly into devices using an integrated USB connector. These drives are typically used to store or transfer personal files, such as photos, videos, music and documents, and to perform data back-up. Integrated 3D NAND enables enhanced storage capacities to store more content.

MicroSD Cards:

Similar to USB flash drives, microSD cards also provide a flash storage repository that enables users to grow their libraries of personal multimedia content. Instead of a USB cable, memory cards are enabled within mobile devices through industry-standard specifications developed by the Secure Digital Association for memory card manufacturers. 3D NAND enables more personal content to be stored.

Mobile Handsets:

Smartphones are the most used mobile devices for connecting to the world through voice, text and the internet, and used for personal entertainment, computing, navigation, transactions, capturing precious moments, and more. 3D NAND will make smartphone use for tomorrow more exciting and compelling, storing larger applications, file sizes and volumes of data.

There are many unique smartphone apps in development today that will make great use of the expanded storage capacities and enhanced performance that 3D NAND provides and includes such new wave capabilities as:

- Holographic Display
- Artificial Intelligence
- Drone Emulation
- High-end Gaming
- Thermal Imaging (night vision)
- Language Translation
- 360° Video

Client SSDs:

3D NAND has already made its way to client SSDs and available on the shelves of retail outlets. Externally connecting to a laptop via a SATA, SAS or PCIe interface, the inclusion of 3D NAND flash provides faster speed, higher capacities and better reliability to handle much larger digital files and multimedia content.

Client SSDs with 3D NAND will also deliver accelerated performance for gaming enthusiasts and creative graphics designers who want to customize their laptops. The addition of 3D NAND provides a simple laptop upgrade path while delivering enhanced endurance and reliability, no-wait boot-up, shorter app load times, and faster data transfer.

3D NAND is especially suited for imaging/removable products, enterprise and client SSDs, and for embedded memory.

Enterprise SSDs:

SSDs enabled with 3D NAND are also making their way to the enterprise in next-generation servers and flash arrays. These drives are designed for business-critical applications requiring ultra I/O performance, terabyte storage capacities, scalability, power efficiency, and high endurance and reliability.

Summary

There is an increasing need for high storage capacity. Due to its performance, power efficiency and reliability, 3D NAND is especially suited for imaging/removable storage products, enterprise and client SSDs, and for embedded memory. For smartphones and other mobile devices with high capacity requirements, 3D NAND storage systems will soon replace 2D NAND, especially in space-constrained devices.

In the computing segment, 3D NAND is a welcome sight for those looking to bridge the gap between performance and capacity. The world's first 64-layer 3D NAND client SSDs are now available, with higher capacities expected in the future.

Additionally, the world's first 3D NAND technology with 96 layers of vertical storage was introduced at Flash Memory Summit 2017. This BiCS4 technology enables higher capacity, performance and reliability versus BiCS2 (48 layers) or BiCS3 (64 layers) and will keep pace with today's escalating storage requirements.

Due to its high bit density, 3D NAND is also cost effective providing low cost per bit ratios. In the coming years, improved 3D NAND capabilities will make it the preferred option for the most demanding storage requirements.