The Linley Group

MICROPROCESSOR report

Insightful Analysis of Processor Technology

WD Rolls Its Own RISC-V Core

Western Digital Opens Superscalar Swerv CPU Source to Others

By Bob Wheeler (February 4, 2019)

Storage vendor Western Digital (WD) has declared independence from licensed CPUs by designing its own RISC-V core. SSD controllers are the first application for its new Swerv EH1 RISC-V CPU. Flash-based products now represent about half its revenue, and WD designs both 3D NAND chips and associated controllers. Over the next several years, it plans to move most of its controller shipments—representing more than one billion CPUs—from licensed to in-house designs. The company has also made the Swerv design available as open source.

Owing to its target application, WD designed the Swerv EH1 as a simple 32-bit real-time core that offers relatively high performance. It implements only the RV32I base ISA plus the multiply and divide (M) and compressed (C) extensions. Its dual-issue in-order pipeline delivers a competitive 5.0 CoreMarks per megahertz. WD completes the core with an instruction cache, tightly coupled memories (TCMs) for instructions and data, an interrupt controller, a debug block, and four 64-bit AXI buses for memory and I/O. Although it aimed for 1.0GHz worst-case operation in TSMC 28nm technology, it achieved 1.8GHz operation in a typical process corner.

The Swerv EH1 is similar to SiFive's new E76 CPU, which achieves slightly lower clock speeds and CoreMarks per megahertz. Last April, WD announced an investment and multiyear license agreement with SiFive, but Swerv is separate from that agreement. Instead, the two companies independently developed dual-issue RISC-V CPUs. Owning Swerv gives WD maximum control over deeply embedded designs. At the same time, it can use third-party RISC-V CPUs or processors (chips) for higher-end products such as storage systems.

Control Over Controllers

WD has numerous reasons for developing Swerv, some technical and others business related. In the former list, it cites 40% performance, 30% power, and 25% area improvements over the unnamed licensed cores (which we believe are Synopsys ARC designs) it currently employs. One issue that straddles the technical and business realms is the ability to add custom ISA extensions without exposing them to an intellectual-property (IP) vendor. In a recent talk, CTO Martin Fink cited open interfaces as the top reason WD chose RISC-V. He believes traditional IP vendors are "locking down" interfaces—that is, making them proprietary. The company wants open coherence fabrics as well as memory and I/O buses. Finally, it's no surprise that a company shipping one billion CPUs would like to eliminate royalties.

Swerv is first appearing in an SSD controller employing a pair of the cores. The main CPU connects with the host interface and processes commands, while the data-path CPU manages the NAND channels and the error-correction engine. WD adds undisclosed custom instructions to accelerate calculations for NAND media handling, which includes functions such as wear leveling, bad-block management, and soft-error recovery. Controllers for USB flash drives must perform similar media handling. The open-source version of Swerv omits these proprietary extensions.

Another contribution WD made to the RISC-V community is a Swerv instruction-set simulator (ISS), which it made available on GitHub in December. The ISS models

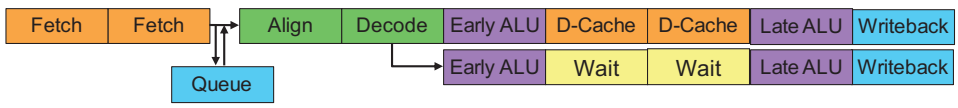

Figure 1. Swerv EH1 pipeline. The addition of late ALUs minimizes load-to-use penalties while avoiding out-of-order-processing complexity.

Price and Availability

Swerv EH1 RTL is freely available now under an Apache 2.0 license online at *github.com/westerndigitalcorporation/swerv*. The Swerv ISS is available online at *github.com/westerndigitalcorporation/swerv-ISS*.

Swerv's memories, interrupts, and debug block. It's useful for design verification and is faster than an RTL simulation.

Fast and Minimalist

WD established its CPU design team in October 2017, with most engineers located in Austin, Texas. Swerv's chief architect spent much of his career designing SPARC processors at Oracle and Sun Microsystems. The team's goal was to design an area- and power-efficient CPU that would run existing firmware faster rather than adding parallelism that would require software changes. The first step beyond the classical five-stage RISC design was adding dual issue to the pipeline. The next step was adding a second (or "late") ALU in each pipe to minimize load-use penalties, a technique Synopsys employed several years earlier in its ARC HS family (see *MPR 11/11/13,* "Synopsys Accelerates ARC CPUs").

The result of these design decisions is an in-order superscalar pipeline with nine stages, shown in Figure 1. The front end consists of two fetch stages, an align stage for compressed instructions, and a decode stage. The first issue slot includes an integer pipe and a load/store pipe, whereas the second slot has an integer pipe and a multiply pipe. A 1-bit-per-cycle divider resides outside the pipeline. To reduce power consumption for large TCMs, the load/store pipe has three cycles to access memory. If an ALU instruction requires the output of a pending load, it proceeds to the late ALUs.

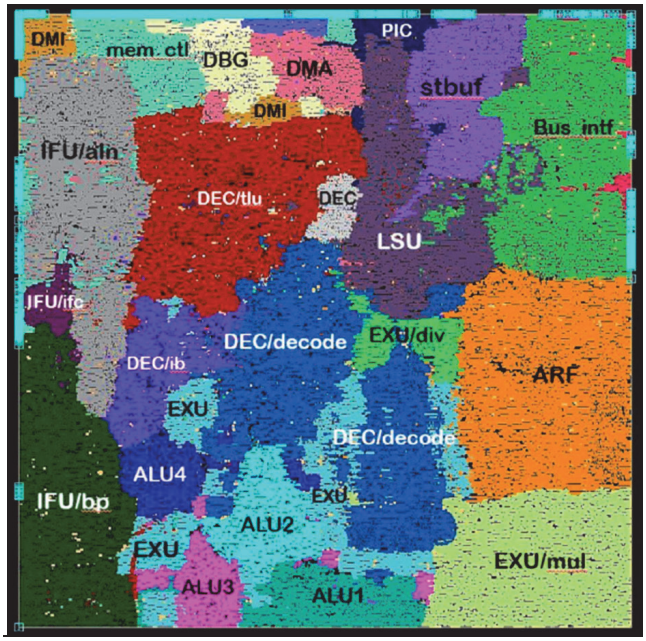

Figure 2. Swerv EH1 physical design. The instruction-fetch unit (IFU) and decode (DEC) logic dominate the left side; the execution unit (EXU), including ALUs, sits at the bottom; and the register file (ARF) resides at right center. The top right comprises the load-store unit (LSU), an associated store buffer (stbuf), and bus interfaces. (Image source: Western Digital)

For branch prediction, Swerv implements the basic Gshare algorithm using a branch history table (BHT) with up to 2,048 entries and a branch target buffer (BTB) with up to 512 entries. The taken-branch penalty is one cycle, whereas the misprediction penalty is four cycles for the primary ALUs and seven cycles for the late ALUs. Although Gshare is simple, it's area efficient, and the company claims it achieves about 96% accuracy for typical embedded code.

The Swerv core provides up to 512KB of tightly coupled instruction and data memory as well as an instruction cache of up to 256KB. The programmable interrupt controller (PIC) supports 15 priorities for up to 255 external interrupts. The load/store unit and instruction-fetch unit each have a 64-bit AXI or AHB-Lite bus-master port. The debug block has its own bus-master port, allowing JTAG access to memory during normal operation. Figure 2 shows the Swerv physical layout (without memories) in TSMC 28nm technology. Synthesized for a 1.0GHz clock speed in a worst-case corner, the core consumes 0.132mm^2. The first internal customer needs only 800MHz, however, reducing area to 0.100mm^2.

Separated at Birth

The SiFive 7 Series represents a superset of Swerv features, including options for 64-bit support, multicore configurations, an MMU, single- and double-precision FPUs, and L2 cache (see *MPR 11/12/18,* "SiFive Raises RISC-V Performance"). The variant closest to Swerv is the 32-bit E76 microcontroller core, although SiFive offers an optional FPU and L2 cache. Otherwise, the cores provide similar capabilities except that Swerv omits the atomic (A) extensions, which are unnecessary in a single-thread design.

The similarities between the Swerv EH1 and 7 Series pipelines are unmistakable. WD uses three data-cache cycles, whereas SiFive uses two, shortening the latter's pipeline to eight cycles. Otherwise, the pipelines are virtually identical, and they yield nearly the same performance. Neither design is silicon proven, but WD appears to offer a small clock-speed advantage.

The Swerv EH1 and the E76 differ in their memory configurations as well. SiFive configures the latter with 32KB of instruction cache and 32KB of instruction and data TCM, although it supports up to 128KB TCMs. The E76 also includes a fast-I/O port that enables low-latency access to dedicated SRAM. We believe the E76 occupies slightly more die area than Swerv, which the addition of atomics could explain.

As Table 1 shows, other licensable 32-bit microcontroller-class CPUs with dual-issue capability include the Arm Cortex-M7 and Synopsys ARC HS44. A member of the second-generation ARC HS family, the HS44 is intended for SSD controllers and other demanding real-time applications (see *MPR 6/12/17,* "Dual-Issue ARC Boosts Performance"). Its deep pipeline enables maximum performance of 11,000 CoreMarks while also handling up to 16MB TCMs for instructions and data. Like its scalar predecessor, the HS44 employs early and late ALUs. ARC Processor Extension tools allow customers to add proprietary instructions. According to our estimate, the HS44 matches Swerv's performance per area.

	Arm Cortex-M7	SiFive E76	Synopsys ARC HS44	WD Swerv EH1
Instruction Set	32-bit Arm v7-M	32-bit RISC-V	32-bit ARCv2	32-bit RISC-V
Max Clock Freq	0.9GHz	1.6GHz†	2.2GHz	1.8GHz
Max IPC	2 IPC	2 IPC	2 IPC	2 IPC
Pipeline Depth	6 stages	8 stages	10 stages	9 stages
CoreMark Perf	5.0CM/MHz	4.9CM/MHz	5.0CM/MHz	5.0CM/MHz
Die Area*	0.11mm²†	0.14mm²†	0.16mm²†	0.13mm²
kCM/mm²	41	56	69	69

Table 1. Dual-issue 32-bit microcontroller-class CPUs. Swerv delivers excellent performance per area, matched only by the larger ARC HS44. All metrics assume TSMC 28nm HP technology. *Without memories and FPU, 12-track library. (Source: vendors, except †The Linley Group estimate)

Cortex-M7's shorter pipeline can't match Swerv's clock speed, but most customers employ the Arm CPU in slower flash-based MCUs anyway (see *MPR 10/6/14,* "Cortex-M7 Doubles Up on DSP"). The M7 offers DSP extensions that the RISC-V designs lack, making the E76 and Swerv less attractive for signal processing. (The RISC-V Foundation is developing a standard set of DSP extensions.) Although the M7 is compact, it delivers only 60% of Swerv's performance per area, according to our estimates.

Risking Independence

The clear loser in WD's plan is Synopsys. It's an early sign the open-source RISC-V movement is hurting traditional CPU-IP suppliers. Among the products for which WD develops its own controllers, a handful of chip designs likely drive most of its CPU volume. These deeply embedded designs have a relatively small and proprietary code base, minimizing software-compatibility concerns in adopting RISC-V.

It's unclear how SiFive arrived at a design that so closely matches Swerv. WD revealed some Swerv details in May 2018, possibly influencing the 7 Series development team. On the other hand, Synopsys preceded both designs with its HS4x, which employs dual integer pipes with early and late ALUs. Regardless, the open-source Swerv EH1 undercuts SiFive's ability to license its basic E76 core. SiFive may be unconcerned, however, as it offers many additional features that Swerv lacks. In fact, WD could be a customer for those more sophisticated cores.

By developing Swerv, WD gained a highly optimized core for its highest-volume chips, giving it maximum control over the design, including opportunities for customization. Eliminating CPU-IP license fees and per-chip royalties should cover development costs. Opening Swerv to others is unlikely to provide the company direct benefits, but its goal is to enable a vibrant RISC-V ecosystem. In the end, WD's decision to develop Swerv appears to be about innovation, time to market, and IP protection rather than a classical make-versus-buy analysis. ♦