Technical Brief

RISC-V: Configurability & Openness for a Data-Centric Computing Architecture

Leveraging Open Standard Interfaces and Customized Chip Design for Big Data and Fast Data Environments

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This document contains forward-looking statements that involve risks and uncertainties, including, but not limited to, statements regarding our product and technology positioning, the anticipated benefits of our new technologies and transitioning into RISC-V open instruction set architectures. Forward-looking statements should not be read as a guarantee of future performance or results, and will not necessarily be accurate indications of the times at, or by, which such performance or results will be achieved, if at all. Forward-looking statements are subject to risks and uncertainties that could cause actual performance or results to differ materially from those expressed in or suggested by the forward-looking statements.

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The Data-Centric World

The majority of discussions about today’s data begin with how it is growing at an exponential rate – doubling every two years and expected to reach hundreds of zettabytes in the next decade.

Data-Centric Data Center Architecture

What’s driving this data-centric world is that the role of data is changing, evolving from just being a record or a log of events, recordings or measurements, to forms of communication that deliver efficiencies in productivity and automation, and ultimately, the value that data delivers becomes a form of currency. Data no longer is just generated from applications, but it now comes from mobile devices, production equipment, machine sensors, video surveillance systems, Internet of Things (IoT) and industrial IoT (IIoT) devices and healthcare monitors to name a few. And, the data that is being generated is created in both large-scale data centers at the “core,” and in remote and mobile sources at the “edge” of the network.

At Western Digital we refer to these classes of data as Big Data and Fast Data environments. Big Data represents very large data sets that may need to be analyzed using computations and algorithms, unmasking trends, patterns, and associations between seemingly disparate data sets. The analysis provides valuable insights and makes new connections that drive precise predictions and decisions that can help to achieve better outcomes. Fast Data environments process or transform data as it is captured, leveraging the algorithms derived from Big Data to provide real-time decisions and results. As Big Data provides insights derived from ‘what happened’ to ‘what will likely happen’ (predictive analysis), Fast Data delivers real-time actions. The data for these environments can come from a host of ‘smart’ machines, environmental monitoring, security and surveillance systems, and securities trading systems that need to act in real-time. To create purpose built architectures for big data and fast data requires a new type of processor.
The current class of general purpose processors are not optimized for these data centric tasks. What is needed is a processor architecture which is open, enables configurability and scales for these data centric applications.

Why RISC-V?

An instruction set architecture (ISA) is the set of machine instructions that comprises the machine language and I/O model of a computer or computing system. It defines everything that a programmer needs to know in order to program it. RISC-V is an open, free ISA which enables a new era of processor innovation. RISC-V is:

- Modular, consisting of base instructions and optional extensions
- Customizable, allowing for custom instructions
- Configurable, enabling flexibility of interfaces and buses to best suit the application

RISC-V instructions are frozen, meaning that software investments will be preserved. Based on its open, modular approach, RISC-V is ideally suited to serve as the foundation of data-centric compute architectures. As Big Data and Fast Data applications start to create more extreme workloads, purpose-built architectures will be required to pick up where today’s general-purpose architectures have reached their limit. Applications which require analytics, machine learning, artificial intelligence and smart systems demand purpose-built architectures.

The key benefits of RISC-V for enabling a new era of data-centric computing architectures include:

1. Independent scaling of resources
2. Open source capabilities
3. Modular chip designs
4. Ability to choose open standard interfaces
Western Digital RISC-V History

Western Digital has been innovating since its founding in 1970. The company has been transforming itself from a storage products company to a provider of data-centric solutions that enable customers to capture, preserve, access and transform an ever-increasing diversity of data. To accelerate this transition, Western Digital has embraced RISC-V and has been part of the RISC-V Foundation since its inception in 2015. Western Digital's support of the RISC-V architecture and contributions to the community help to accelerate development of special-purpose processors designed to meet the needs of Big Data and Fast Data applications. As Big Data gets bigger and faster, and Fast Data gets faster and bigger, the "one size fits all" approach of general-purpose computing is failing to meet the increasingly diverse application workloads of our data-centric world.

Accelerating the RISC-V Ecosystem

As with any open source initiative, RISC-V needs a complete ecosystem surrounding it in order to thrive. The components of the ecosystem can be very diverse, yet the power of open source contributions can accelerate the build out. Whether it is software, hardware, operating systems, firmware, drivers, etc. each of these components is important to ensure the success of RISC-V. To help encourage innovation in the ecosystem, Western Digital has made several recent contributions to the community. This includes recent contributions to the upstream Linux kernel that helped Linux distributions, such as Fedora, to support RISC-V hardware. Now RISC-V can be utilized to run Fedora Linux. This enables software and firmware engineers to develop applications, middleware, tools, etc so they will run on Linux via RISC-V processors. Further details are available at https://github.com/westerndigitalcorporation/RISC-V-Linux.

In addition, Western Digital is focusing on RISC-V hardware development, announcing in 2017 that it would gradually transition its core, processor, and controller development to RISC-V designs. Most of the RISC-V cores presently being developed are planned for use in embedded designs for flash controllers, SSDs, etc. To help accelerate the build out of the RISC-V ecosystem, Western Digital has open sourced its first RISC-V core. The Western Digital SweRV Core™ EH1 is a 32-bit, 2-way superscalar, 9 stage pipeline core. Western Digital is providing the SweRV Core to the open source community for everyone to utilize and contribute to. Although the SweRV Core is an in order execution core, it's relative single core performance exceeds that of many out of order cores.
With an expected simulation performance of up to 5.0 CoreMark/Mhz and small footprint, it offers compelling capabilities for embedded devices supporting data-intensive edge applications, such as industrial IoT, real-time analytics in surveillance systems, and other smart systems. We are excited to see the various implementations the marketplace will create based on this new core. Obtain the SweRV Core EH1 now at https://github.com/westerndigitalcorporation/swerv_eh1.

Western Digital has also created an instruction set simulator (ISS) for RISC-V. The SweRV ISS was developed independently from the SweRV Core to ensure RISC-V cores are executing instructions properly. The SweRV ISS models closely coupled memories, caches, interrupts and more. Western Digital utilized it to debug and verify the SweRV Core and it can be used to validate your RISC-V core. Download the SweRV ISS at https://github.com/westerndigitalcorporation/swerv-ISS.

SweRV ISS™


Estimated simulation performance based on internal Western Digital results; NOT actual comparison to CoreMark testing results
Western Digital is passionate about open standard interfaces. We acknowledge that general purpose architectures which leverage proprietary interfaces are useful for a broad range of applications. But the data-centric and memory-centric purpose-built solutions which Western Digital is creating require open standard interfaces. The growth and popularity of the NVMe-over-Fabric (NVMf) showcases how an open standard can unleash innovation. Western Digital believes that an open memory standard interface can similarly enable unique purpose-built solutions.

One example of memory innovation could be leveraged around cache coherency. This ensures that multiple processors that are sharing cache memory are in sync. Cache coherency enables compute power to scale as additional processors are added. Western Digital recently partnered with SiFive to introduce OmniXtend™. It’s an open, innovative cache coherence over an ethernet network standard for multiprocessors that leverages the openness and configurability of RISC-V to move compute closer to data and deliver new possibilities to memory-centric architectures. OmniXtend provides a routable and switchable connection through fabric of compute, memory, I/O, and current and future storage technologies. OmniXtend is an open proposed standard that utilizes the 802.3 physical interface. This ubiquitous interface enables cache coherence fabric architectures to be built cost effectively, allowing for new innovations in memory-centric network architectures. Western Digital hopes that OmniXtend will open the door for further fabric-attached innovation. For further details, go to https://github.com/westerndigitalcorporation/omnixtend.
Looking Ahead

To realize the possibilities of data, we need to capture, preserve, access, and transform it to its full potential. Big Data and Fast Data environments in the core, and at the edge, have exceeded the capabilities of general-purpose compute architectures. The extreme data-centric environments of tomorrow’s applications require purpose-built environments that support independent scaling of data transformation resources in an open manner.

Western Digital is committed to the mission of the RISC-V Foundation and its ecosystem, and together, we can create environments for data to thrive. When data thrives, our people, communities and planet can thrive, all through the power, potential and possibilities of data.

About Western Digital

Western Digital creates environments for data to thrive. The company is driving the innovation needed to help customers capture, preserve, access and transform an ever-increasing diversity of data. Everywhere data lives, from advanced data centers to mobile sensors to personal devices, our industry-leading solutions deliver the possibilities of data. Western Digital™ data-centric solutions are marketed under the G-Technology™, SanDisk®, Upthere™ and WD® brands.

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