

The Journey of RISC-V Implementation

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In this article, Western Digital's Ted Marena explores the reasons companies have and the process they go through when integrating the open process instruction set architecture RISC-V.

The open processing instruction set architecture (ISA) known as RISC-V is quickly becoming mainstream. However, there are many individuals who are not aware of why it is so compelling. Others have heard of RISC-V but only on a surface level. As I've talked to numerous individuals about why they have chosen RISC-V, the reasons are varied but each person seems to have gone on a similar journey. Depending on your awareness and current use of RISC-V, you are likely to be able to relate to this article. I have been fortunate to be part of two organizations which have made the decision to move to RISC-V.

Most people start out becoming aware of RISC-V from someone they know or through the RISC-V Foundation. The RISC-V Foundation was set up in 2015 to protect the ISA, manage its specifications, and promote RISC-V broadly. Whether you first learned of RISC-V from an event, a technical article, a meetup or a co-worker, your initial reaction was probably something like are you crazy? The thinking usually centers around "we already have processors and don't need another one!" Personally, this was my first reaction and many others' I've spoken with as well.

The Value Proposition of RISC-V

Once you take the time to listen to the reasons and compelling value propositions of RISC-V, it is clear why the technology has been experiencing tremendous growth. It is interesting that there are numerous reasons companies are moving to RISC-V. Here are some of the more common responses:

- Frozen ISA – software written for RISC-V will run forever on an equivalent RISC-V core. This preserves software investments.
- The equivalent of having a microarchitecture license enables differentiation.
- The ability to innovate the processor architecture for a purpose-built device/solution.
- Increased security given the clean slate afforded by RISC-V.
- Allowing software teams to more heavily influence the hardware.

For Western Digital, RISC-V and the expansion of open-source innovation is key to enabling the purpose-built computing environments necessary to meet the demands of data-centric applications such as artificial intelligence (AI), machine learning, analytics, and smart system. The company realized that, as data continued to grow exponentially, the "general-purpose" technologies and architectures that have been in place for decades were reaching their limits of scalability, performance, and efficiency. Additionally, general-purpose workloads typically have a uniform ratio of processing resources, such as operating system (OS) processing, specialty

offload processing, memory, data storage and interconnect. This “one size fits all” approach of computing was failing to meet the increasingly diverse application workloads of our data-centric world. As the diversity of Big Data and Fast Data workloads continued to expand, data-centric compute architectures needed the ability to scale resources independent of one another.

RISC-V Utilization Example: Western Digital

As the company was an initial member of the RISC-V Foundation in 2015, RISC-V seemed like a possible solution. The CTO organization began exploring using RISC-V for purpose-built, data-centric applications. Much of this work was done in 2016. As the RISC-V membership continued to grow, Western Digital realized that if they were to move to the technology then the ecosystem needed to be built up. Towards the fall of 2017, the decision was made to go all-in with RISC-V. At the 7th RISC-V workshop in Milpitas, CA, Western Digital underscored its commitment to RISC-V initiative, announcing their plans in a keynote address to transition their own consumption of cores, which was over a billion, to RISC-V. This was the most significant commitment to the RISC-V initiative by a technology leader up to that point. This move by Western Digital was a huge step forward for the initiative, accelerating the advancement of the technology and the surrounding ecosystem.

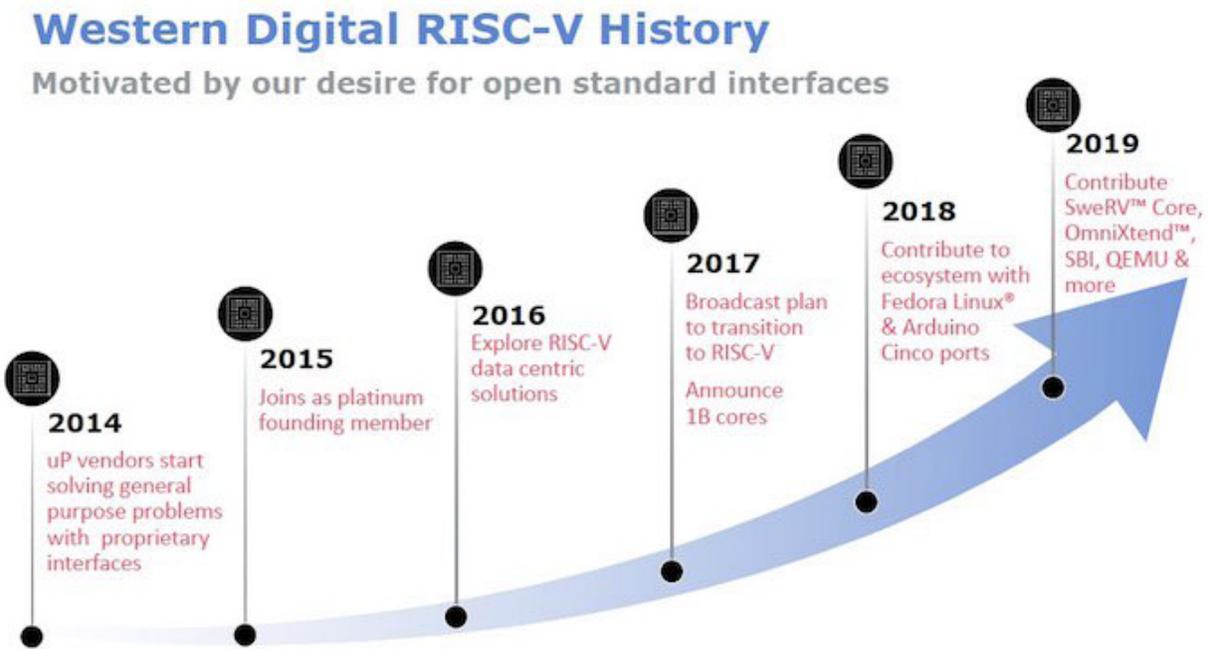


Figure 1. RISC-V History

In 2018, an experienced CPU development team was hired. This group set off to design Western Digital’s first RISC-V Core. In January 2019, the SweRV Core EH1 was introduced. It is a 32 bit, 9 stage pipeline, dual superscalar architecture which offers compelling performance for embedded applications. The SweRV Core was donated to the open-source community to accelerate the RISC-V ecosystem. In addition to the RISC-V CPU development team, Western

Digital has also dedicated numerous software engineers to assist with building out the RISC-V ecosystem. Contributions have been made including [Supervisory Binary Interface \(SBI\)](#), [QEMU support](#), an [abstraction layer firmware](#) package, [among other activities](#).

Based on feedback and suggestions from the open-source community, Western Digital enhanced the [SweRV Core EH1 version 1.1](#). The company will be integrating the SweRV Core into an SoC which will be used in a non-volatile storage device in 2020. In addition, other developments based on the SweRV Core will be done in the [CHIPS Alliance group](#), whose members include Western Digital, Google, SiFive, Alibaba and many others. CHIPS Alliance is an organization created to develop RTL hardware for SoCs, chiplets, and complex peripherals as well as open-source development tools. By creating an open and collaborative environment, CHIPS Alliance shares resources to lower the cost of development. CHIPS Alliance is open to all organizations who are interested in developing open-source hardware or software tools to accelerate the creation of more efficient and innovative chips.

RISC-V Utilization Example: Microchip

The decision process and development efforts for other organizations using RISC-V is similar but unique in other ways. For example, Microchip Technology was an early adopter of RISC-V in late 2018 when it announced its [PolarFire® SoC architecture](#), the world's first RISC-V based SoC FPGA. Its evaluation of RISC-V began in late 2014, and it became a founding member of the RISC-V Foundation as Microsemi — prior to the company's acquisition by Microchip. As the FPGA Business Unit was deciding on what type of processor should be used for PolarFire SoC, discussion initially leaned toward traditional processor cores. The conclusion was to adopt RISC-V as the benefits of the open ISA became clear. This decision allowed Microchip to architect a unique processor subsystem that could run Linux® and real-time very deterministically.

These two company examples that chose RISC-V demonstrates that calculated risks can lead to significantly better outcomes. RISC-V technology can play that role in helping organizations innovate, differentiate, and improve their product portfolio.

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