Serial ATA—Next Generation Storage Interface

Why Do We Need a New Interface?

Limitations of Parallel ATA

Serial ATA was designed to overcome a number of limitations of Parallel ATA. The most significant limitation of Parallel ATA is the difficulty in increasing the data rate beyond 100 MBytes/s. Parallel ATA uses a single-ended signaling system that is prone to induced noise. Increasing the Parallel data rate beyond 100 MBytes/s would require a new signaling system that would not be backward compatible with existing systems. Hard disk drives, such as the Deskstar® 7K500, 7K250 and 7K80 as well as the Travelstar® 7K100 and 5K100 series currently outrun the 100 MByte/s data transfer rate. As a result, a new interface system has been defined to accommodate the faster processing capabilities of next generation high-speed desktop, notebook and entry-server architectures.

Serial ATA has emerged as the industry standard internal storage interface designed to solve the bandwidth constraints of Parallel ATA, as well as well as the dependence on 5V signaling lines that are incompatible with silicon processes used in a wide variety of microprocessors. Serial ATA overcomes these issues by employing a 250mV differential signaling method. Differential signaling rejects induced noise. The 250mV differential signal level is compatible with future microelectronic fabrication processes.

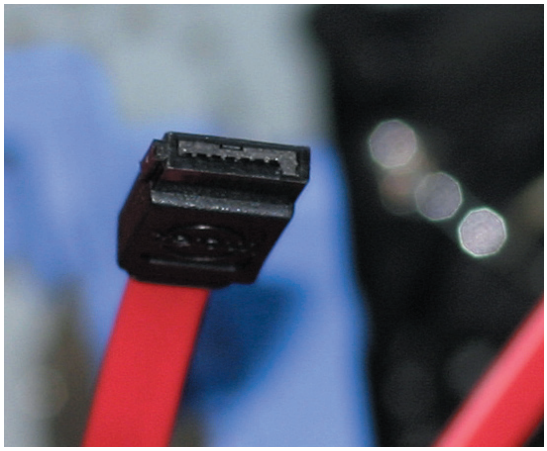

Figure 1: Serial ATA Interface

Forecasts indicate ATA dominance

ATA is the dominant HDD interface in the industry. The ATA interface market is expected to be approximately 190 million units in 2003, accounting for about 90% of all HDDs shipped, according to International Data Corporation's (IDC) 2002/03 forecasts. By 2006, IDC projects ATA unit shipments will increase to beyond 310 million and continue to account for 90% of all HDDs shipments. It is clear that the market will demand ATA-class HDDs for the foreseeable future.

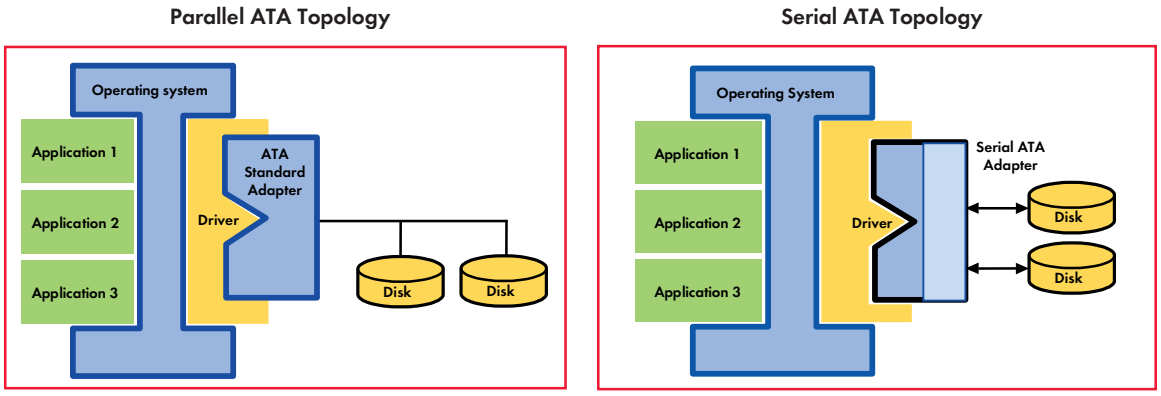

Figure 2: Parallel ATA and Serial ATA Topologies

Serial ATA standards activities

The Serial ATA Working Group published the Serial ATA 1.0a specification in 2003, which was in turn adopted by the ANSI T13 public standards committee as the ATA/ATAPI-7 V3 specification. In 2004, the Serial ATA Working Group evolved into a formal organization called the Serial ATA International Organization (SATA-IO), dedicated to sustain the specification and create further SATA-based interface solutions. The pioneering work instigated by the Serial ATA Working Group and carried forward by SATA-IO has resulted in a number of extensions to the basic Serial ATA 1.0a specification, including both interface transfer rate solutions of 1.5 Gb/second and 3.0 Gb/second, as well as optional features such as Native Command Queuing, Asynchronous Notification, Staggered Spin-Up, Hot Plugability, Link Power Management™, new cabling configurations, Port Multiplier, Port Selector, and ClickConnect to name a few. As of March, 2005, SATA-IO has grown to over 100 members, and HGST was elected to the SATA-IO Board of Directors.

Serial ATA Features and Specifications

The basics

Serial ATA is designed to be transparent to the host system software layer which allows existing operating systems, device drivers and applications to run without modification. The interface is a 4-wire, point-to-point configuration—supporting one device per controller connection. Thus, there are no master/slave configuration jumper issues as there are with Parallel ATA drives. The SATA interface provides a substantial reduction in pin count from Parallel ATA, and a smaller cable configuration which both facilitates air flow as well as improves cable routing.

Layering model

The Serial ATA function is divided into four layers, as shown in Table 1. The Transport and Link layers control overall operation. The Application layer is designed to appear identical to Parallel ATA, thereby maintaining software compatibility. The Physical layer handles the high speed serial communications between the host and device.

Serial ATA can transport all ATA and ATAPI protocols, and is designed to be forward compatible with future ATA and SATA standards.

4	**Application**
3	**Transport**
2	**Link**
1	**Physical**

Table 1: Serial ATA Communications Layer Model

Physical layer

The Serial ATA physical layer (PHY) uses low-voltage (250mV) differential signaling to enable speeds of 1.5Gb/s and beyond. The roadmap is designed to carry the interface for 10 years, through 6.0Gb/s. There are two differential pairs, one for transmit and one for receive. The PHY layer incorporates serializer/deserializer, provides out of band (OOB) signaling, and handles power-on sequencing and speed negotiation. Transmit Data is serialized from 10-bit characters, and Receive Data is deserialized to 10-bit characters. Device status feedback is provided to the to the link layer.

The interface supports both cabled (1 and 2 meter lengths) as well as back-plane connections. The connectors are designed to blind mate, and staggered contacts are provided to facilitate hot plugging. There are three power supply voltages: 12V, 5V and 3.3V. The first generation cables and connectors are designed to support 3.0Gb/s speed. The connector location and interface is common for 3.5- and 2.5-inch devices, facilitating the ability to support multiple form factors within a single bay.

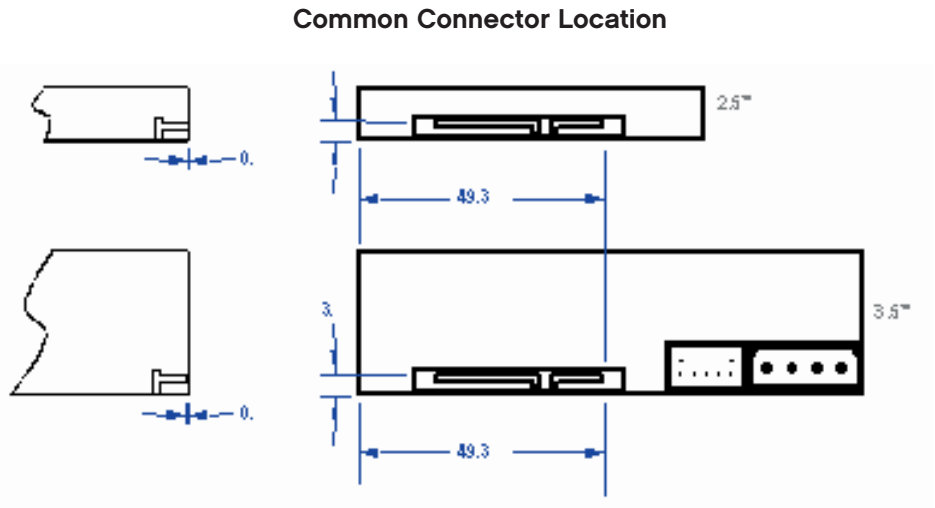

Figure 3: Common Connector Location

Link layer

The Link layer is responsible for sending and receiving frames, control signal primitives and performing flow control. The Link layer contains a primitive character encoder/decoder, 8B/10B encoder/decoder, 32-bit CRC calculator, data scrambler/descrambler and a layer controller.

Transport layer

The Transport layer handles the packing and unpacking of ATA and ATAPI information into Frame Information Structures. The Transport layer also manages the FIFO or buffer memory for controlling data flow.

Application layer

The Application layer interacts with the Transport layer through a register interface that is equivalent to that presented by a traditional Parallel ATA host adapter. A shadow register block is defined that is both compatible with Parallel ATA and anticipated future extensions. Software is thus backward compatible with Parallel ATA devices.

Serial ATA Opportunities

The opportunity for Serial ATA architectures transcends hard disk drives and host bus adapters, and encompasses all ATA devices attached to the system bus. The key to rapid adoption is widespread industry support. The introduction of Serial ATA support in Intel chipsets is the most significant step toward the industry adoption of Serial ATA HDDs.

At the initial stages, hard disk drives which support the Serial ATA 3.0 Gb/s interface will be best suited for entry server and the high-end desktop markets, with 1.5 Gb/s SATA mobile drives appearing in early notebook PCs. Ultimately Serial ATA should permeate the entire Parallel ATA market. This will require costs dropping enough to replace Parallel ATA in non-HDD applications where the interface performance demands are not as critical, such as from optical and DVD drives. Eventually SATA performance features and benefits could encroach on markets currently served by other interface solutions like parallel SCSI. For example, Parallel ATA implementations are already seen in single user low-end workstation products. Integrators in these entry enterprise markets including low-end workstations, entry server and NAS may find Serial ATA an attractive architecture solution.

The Serial ATA interface is an important technology upgrade to the Parallel ATA interface. Serial ATA advantages include the following:

- Point to point connection which eliminates Master/Slaveconfigurations
- Thinner and longer cables
- Continuity in software drivers—SATA hard disk drives are compatible
- Low differential voltage signals
- Robust migration path for interface performance—bandwidth today defined at 150, 300 and 600 MBytes/s
- Improved connection design to accommodate hot-plug and blind mate applications
- 32 bits CRC error checking on all data and control information
- References and specifications

For more information and the latest specifications, please refer to the Serial ATA website at www.SATA-IO.org. For more information on HGST Serial ATA product offerings, please visit our website at www.hgst.com/products.

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