Western Digital

Product Manual

Ultrastar® DC HA340

3.5-inch Serial ATA Hard Disk Drive

Models: WUS721208BLE604
                WUS721206BLE604
                WUS721204BLE604

                WUS721208BLE6L4
                WUS721206BLE6L4
                WUS721204BLE6L4

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1 General

1.1 Introduction

This document describes the specifications of the Western Digital Ultrastar® DC HA340 3.5-inch 7200-rpm serial ATA interface hard disk drive with the following model numbers:

Table 1 R/N and Models

Capacity[1]	Type	Interface	Format	Model#	Security Mode	P3 Power Disable Supported
8TB	3VAHA2	Serial ATA	512 Emulation	WUS721208BLE604	Base (SE)	Yes
				WUS721208BLE6L4		No
6TB	3VAHA2			WUS721206BLE604	Base (SE)	Yes
				WUS721206BLE6L4		No
4TB	3VAHA2			WUS721204BLE604	Base (SE)	Yes
				WUS721204BLE6L4		No

[1] One TB equals one trillion bytes. Actual user capacity may be less due to operating environment.

How to Read Model Number Format

WUS721208BLE604 - 8TB SATA 6Gb/s 512e Base (SE) with Legacy Pin 3 configuration

W = Western Digital
U = Ultrastar
S = Standard
72 = 7200 RPM
12 = Max capacity in series (12TB)
08 = Capacity of this model (8TB)
B = Generation code
L = 26.1 mm z-height
E6 =   Interface (512e SATA 6Gb/s)
y =   Power Disable Pin 3 status
        0 = Power Disable Pin 3 support,
        L = Legacy Pin 3 configuration – No Power Disable Support
z =   Data Security Mode
        4 = Base (SE)**: No Encryption, Sanitize Overwrite only

** ATA Security Feature Set comes standard on SATA

1.2   Glossary

ADM   Automatic Drive Maintenance
DFT   Drive Fitness Test
ADM   Automatic Drive Maintenance
GB   1,000,000,000 bytes
Gbps   1,000,000,000 bits per second
KiB   1,024 bytes
Kbpi   1,000 bits per inch
Ktpi   1,000 tracks per inch
MiB   1,048,576 bytes
MB   1,000,000 bytes
MB/s   1,000,000 bytes per second
Mbps   1,000,000 bits per second
MiB/s   1,048,576 bytes per second
PI   Protection Information
PSID   Physical presence Security ID
S.M.A.R.T.   Self-Monitoring Analysis and Reporting Technology
SE   Secure Erase

1.3   General Caution

Do not apply force to the Top cover. Handle the drive by its edges or the frame only.

Do not touch the interface connector pins or the surface of the printed circuit board.

The drive can be damaged by shock or ESD (Electrostatic Discharge). Any damage sustained by the drive after removal from the shipping package and opening the ESD protective bag are the responsibility of the user.

1.4   References

- Serial ATA II: Extensions to Serial ATA 1.0
- Serial ATA International Organization: Serial ATA Revision 3.5

2   General Features

- Data capacity of up to 8TB
- Spindle speed of 7200 RPM
- Fluid dynamic bearing motor
- Dual stage actuator (DSA)
- Closed-loop actuator servo
- Load/unload mechanism, non-head disk contact start/stop
- Automatic actuator lock
- Write cache
- Power saving modes/low RPM idle mode (APM)
- S.M.A.R.T. (Self-Monitoring and Analysis Reporting Technology)
- Adaptive zone formatting
- RVS (Rotational Vibration Safeguard)
- 256 MiB DDR3 Memory
- Segmented buffer implementation
- Automatic error recovery procedures for read and write commands
- Automatic defect reallocation
- Power Disable (SATA)
- PSID support
- Sector format of 512e bytes/sector
- Native command queuing support
- Self-diagnostics at Power on
- Serial ATA data transfer 6/3/1.5 Gbps
- CHS and LBA modes
- Security feature support
- 48 bit addressing feature
- SATA 3.5 compliant with optional SATA 3.3 Power Disable Feature support

Part 1. Functional Specification

3 Fixed Disk Subsystem Description

3.1 Control Electronics

The drive is electronically controlled by a microprocessor, several logic modules, digital/analog modules, and various drivers and receivers. The control electronics perform the following major functions:

- Controls and interprets all interface signals between the host controller and the drive.
- Controls read write accessing of the disk media, including defect management and error recovery.
- Controls starting, stopping, and monitoring of the spindle.
- Conducts a power-up sequence and calibrates the servo.
- Analyzes servo signals to provide closed loop control. These include position error signal and estimated velocity.
- Monitors the actuator position and determines the target track for a seek operation.
- Controls the voice coil motor and secondary actuator drivers to align the actuator in a desired position.
- Constantly monitors error conditions of the servo and takes corresponding action if an error occurs.
- Monitors various timers such as head settle and servo failure.
- Performs self-checkout (diagnostics).

3.2 Head Disk Assembly

The head disk assembly (HDA) is assembled in a clean room environment and contains the disks, a spindle motor, actuator assembly, and voice coil motor. Air is constantly circulated and filtered when the drive is operational. Venting of the HDA is accomplished via a breather filter.

The spindle is driven directly by a brushless, sensorless DC drive motor. Dynamic braking is used to stop the spindle quickly.

3.3 Actuator

The read/write heads are mounted in the actuator. The actuator is a swing-arm assembly driven by a voice coil motor. A closed-loop positioning servo controls the movement of the actuator. An embedded servo pattern supplies feedback to the positioning servo to keep the read/write heads centered over the desired track.

The actuator assembly is balanced to allow vertical or horizontal mounting without adjustment.

When the drive is powered off, the actuator automatically moves the head to the actuator ramp outside of the disk where it parks.

4 Drive Characteristics

This section describes the characteristics of the drive.

4.1 Default Logical Drive Parameters

The default of the logical drive parameters in Identify Device data is as shown below.

Table 2   Formatted Capacity

Description	SATA model		
Physical Layout			
Label capacity	8TB	6TB	4TB
Bytes per Sector	512e	512e	512e
Number of Heads	8	6	5
Number of Disks	4	3	3
Logical Layout[1]			
Bytes per Sector	512	512	512
Number of Sectors	15,628,053,168	11,721,045,168	7,814,037,168
Total Logical Data Bytes	8,001,563,222,016	6,001,175,126,016	4,000,787,030,016

Notes:

[1] Logical layout: Logical layout is an imaginary drive parameter (that is, the number of heads) which is used to access the drive from the system interface. The Logical layout to Physical layout (that is, the actual Head and Sectors) translation is done automatically in the drive. The default setting can be obtained by issuing an IDENTIFY DEVICE command.

4.2 Data Sheet

Table 3 Data sheet

Description	8TB SATA Model	6TB SATA Model	4TB SATA Model
Max data transfer rate (Mbps)	2280	2256	2208
Max interface transfer rate (MB/s)	600	600	600
Typical max sustained transfer rate (MB/s)	285	282	276
Typical max sustained transfer rate (MiB/s)	271	269	263
Data buffer size (MiB)	256	256	256
Rotational speed (RPM)	7200	7200	7200
Recording density- max (kbpi)	2059	2059	2059
Track density - nominal (ktpi)	493	493	400
Areal density - max (Gbits/in^2)	1022	1022	834

4.3 World Wide Name Assignment

Table 4 World Wide Name Assignment

Description	SATA Model
Organizationally Unique Identifier (OUI)	0014EEh (for Western Digital)
SHBU Block Assignment (Initial)	2h (Thailand)

4.4 Drive Organization

4.4.1 Drive Format

Upon shipment from WESTERN DIGITAL manufacturing, the drive satisfies the sector continuity in the physical format By means of the defect flagging strategy described in *Section 5 "Defect Flagging Strategy"* in order to provide the maximum performance to users.

4.4.2 Cylinder Allocation

Physical cylinder is calculated from the starting data track of 0. It is not relevant to logical CHS. Depending on the capacity some of the inner zone cylinders are not allocated.

Data cylinder
This cylinder contains the user data which can be sent and retrieved via read/write commands and a spare area for reassigned data.

Spare cylinder
The spare cylinder is used by Western Digital manufacturing and includes data sent from a defect location.

4.5   Performance Characteristics

Drive performance is characterized by the following parameters:

- Command overhead
- Mechanical positioning
  - Seek time
  - Latency
- Data transfer speed
- Buffering operation (Look ahead/Write cache)

All the above parameters contribute to drive performance. There are other parameters that contribute to the performance of the actual system. This specification defines the characteristics of the drive, not the characteristics of the system throughput which depends on the system and the application.

The terms "Typical" and "Max" are used throughout this specification with the following meanings: Typical. The average of the drive population tested at nominal environmental and voltage conditions. Max. The maximum value measured on any one drive over the full range of the environmental and voltage conditions. (See *Section 6.2 "Environment"* and *Section 6.3, "DC Power Requirements"*).

4.5.1   Mechanical Positioning

4.5.1.1   Average Latency

Table 5   Latency Time

Rotational Speed	Time for a Revolution (ms)	Average Latency (ms)
7200 RPM	8.33	4.16

4.5.2   Drive Ready Time

Table 6 Drive Ready Time

Power on to Ready	Typical (sec)	Maximum (sec)
8TB Model	11.59	11.87

Drive Ready   The condition in which the drive is able to perform a media access command (such as read, write) immediately.

Power on   This includes the time required for the internal self-diagnostics.

Notes: The typical and maximum drive ready times in the table are for proper power shutdown using the required power-off sequence. The actual time may vary depending on the drive pre-condition before the EPO event.

4.5.3   Operating Modes

4.5.3.1   Operating Mode Descriptions

Operating Mode	Description
Spin up	Period of time from 0 rpm to full rpm
Start up	Period of time from power on to drive ready
Seek	Seek operation mode
Write	Write operation mode
Read	Read operation mode
Active	Drive is able to perform a media access command (such as read, write) immediately
Idle_0	Drive Ready, not performing I/O; drive may power down selected electronics to reduce power without increasing response time
Idle_A	Drive Ready, not performing I/O; drive may power down selected electronics to reduce power without increasing response time
Idle_B	Spindle rotation at 7200 RPM with heads unloaded
Idle_C/Standby_Y	Spindle rotation at low RPM with heads unloaded
Standby_Z	Actuator is unloaded and spindle motor is stopped. Commands can be received immediately
Sleep (SATA)	Actuator is unloaded and spindle motor is stopped. Only soft reset or hard reset can change the mode to Standby_Z

Note: Upon power down or spindle stop a head locking mechanism will secure the heads in the OD parking position.

4.5.3.2   Mode Transition Times

Mode transition times are shown below.

Table 7   Mode Transition Times

From	To	RPM	Typical (sec)
Idle_B	Active	7200	1
Idle_C	Active	6300 --> 7200	4
Standby_Y	Active	6300 --> 7200	4
Standby_Z	Active	0 --> 7200	15

Note: Maximum transition time of 30 seconds based on drive timeout value.

5   Defect Flagging Strategy

Media defects are remapped to the next available sector during the Format Process in manufacturing. The mapping from LBA to the physical locations is calculated by an internally maintained table.

5.1   Shipped Format

- Data areas are optimally used.
- No extra sector is wasted as a spare throughout user data areas.
- All pushes generated by defects are absorbed by the spare tracks of the inner zone.

Figure 1   PList physical format

	N	N+1	defect	N+2	defect	N+3	

skip   skip
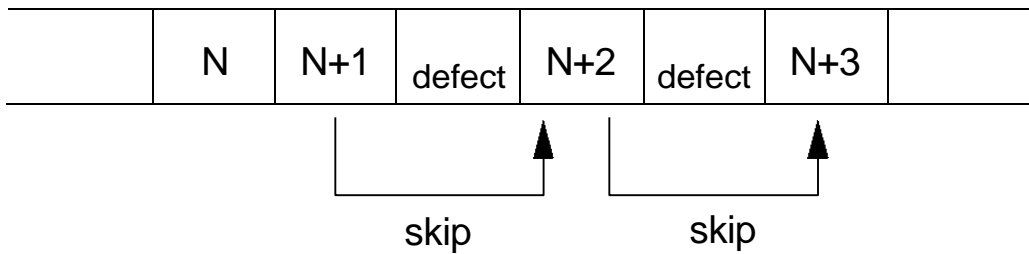
Defects are skipped without any constraint, such as track or cylinder boundary.   The calculation from LBA to physical is done automatically by internal table.

6 Specification

6.1 Electrical Interface

6.1.1 Connector Location

Refer to the following illustration to see the location of the connectors.

Figure 2 Connector location
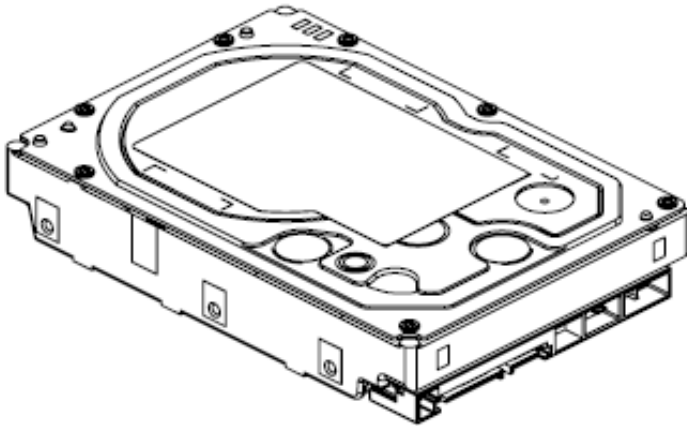
Figure 3 Connector pin assignments
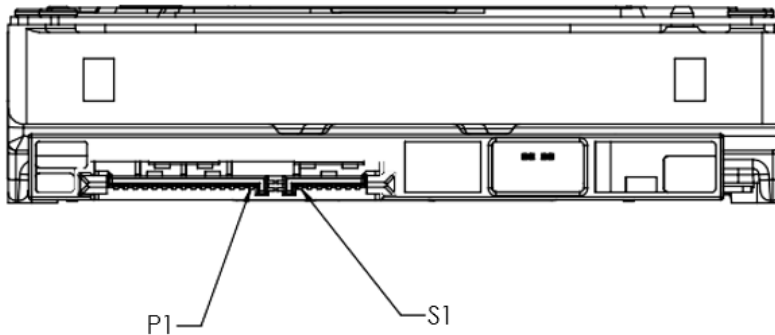
6.1.1.1 Signal Connector (SATA)

A Serial ATA device may be either directly connected to a host or connected to a host through a cable.

For direct connection, the device plug connector is inserted directly into a backplane connector. The device plug connector and the backplane connector incorporate features that enable the direct connection to be hot pluggable and blind mated.

For connection via cable, the device signal plug connector mates with the signal cable receptacle connector on one end of the cable. The signal cable receptacle connector on the other end of the cable is inserted into a host signal plug connector. The signal cable wire consists of two twinax sections in a common outer sheath.

Besides the signal cable, there is also a separate power cable for the cabled connection. A Serial ATA power cable includes a power cable receptacle connector on one end and may be directly connected to the host power supply on the other end or may include a power cable receptacle on the other end. The power cable receptacle connector on one end of the power cable mates with the device power plug connector. The other end of the power cable is attached to the host as necessary.

6.1.2 Signal Definition (SATA)

SATA has receivers and drivers to be connected to TX+/- and RX +/- Serial data signal.
Defines the signal names of I/O connector pin and signal name.

Table 8   Interface Connector Pins and I/O Signals

	No.		Plug Connector Pin Definition	Signal	I/O
Signal	S1	GND	2nd mate	Gnd	
	S2	A+	Differential signal A from Phy	RX+	Input
	S3	A-		RX-	Input
	S4	Gnd	2nd mate	Gnd	
	S5	B-	Differential signal B from Phy	TX-	Output
	S6	B+		TX+	Output
	S7	Gnd	2nd mate	Gnd	
			Key and spacing separate signal and power segments		
Power	P1	Reserved*	NOT USED (P1 and P2 tied internally)	Reserve	
	P2	Reserved*	Not USED (P1 and P2 tied internally)	Reserve	
	P3	Reserved* or PWDIS* (option)	Not USED (P1, P2 and P3 tied internally) or Enter/Exit Power Disable (option)	Reserve or PWDIS	
	P4	Gnd	1st mate	Gnd	
	P5	Gnd	2nd mate	Gnd	
	P6	Gnd	2nd mate	Gnd	
	P7	V5	5V power,pre-charge,2nd Mate	5V	
	P8	V5	5V power	5V	
	P9	V5	5V power	5V	
	P10	Gnd	2nd mate	Gnd	
	P11	Reserved	Support staggered spin-up and LED activity VDih max=2.1V	Reserve	
	P12	Gnd	1st mate	Gnd	
	P13	V12	12V power,pre-chage,2nd mate	V12	
	P14	V12	12V power	V12	
	P15	V12	12V power	V12	

* SATA Specification Revision 3.1 and prior revisions assigned 3.3V to pins P1, P2, and P3. In addition, device plug pins P1, P2, and P3 were required to be bused together. In the standard configuration of this product, P3 is connected with P1 and P2 and this product behaves as SATA 3.1 or prior version product in a system designed to SATA 3.2 system that does not support the 3.3 feature. For product with the optional SATA 3.3 Power Disable Feature supported, P3 is now assigned as the POWER DISABLE CONTROL PIN. If P3 is driven HIGH (2.1V-3.6V max), power to the drive circuitry will be disabled. Drives with this optional feature WILL NOT POWER UP in systems designed to SATA Spec Revision 3.1 or earlier because P3 driven HIGH will prevent the drive from powering up.

6.1.2.1   TX+ / TX-

These signals are the outbound high-speed differential signals that are connected to the serial ATA cable.

6.1.2.2   RX+ / RX-

These signals are the inbound high-speed differential signals that are connected to the serial ATA cable.

6.1.2.3   5V PRECHARGE

+5 Vdc that is available on the extended pins. It is used for PRECHARGE when connected to backplane incorporated feature.

6.1.2.4   12V PRECHARGE

+12 Vdc that is available on the extended pins. It is used for PRECHARGE when connected to backplane incorporated feature.

6.1.3   Out-of-Band Signaling (SATA)

Figure 4   The timing of COMRESET, COMINIT and COMWAKE
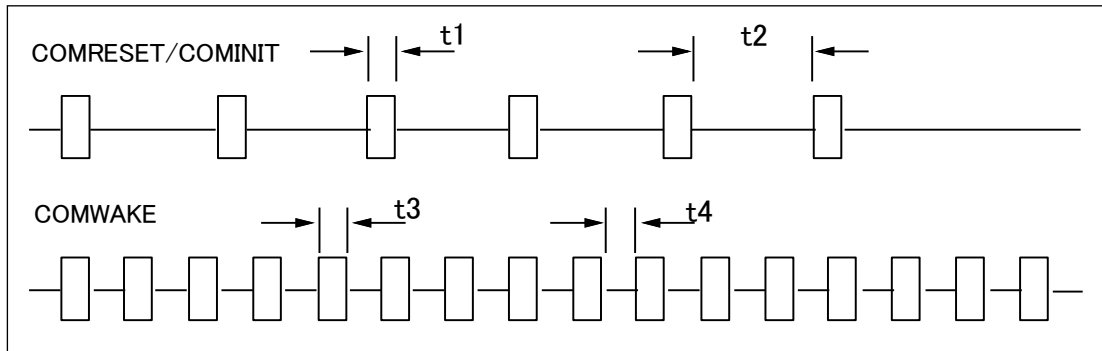
Table 9   Parameter descriptions

	PARAMETER DESCRIPTION	Nominal (ns)
t1	ALIGN primitives	106.7
t2	Spacing	319.9
t3	ALIGN primitives	106.7
t4	Spacing	106.5

6.1.4   Voltage and Ground Signals

The 12V and 5V contacts provide all of the voltages required by the drive. The two voltages share a common ground plane to which all of the ground contacts are connected.

6.1.5   Ready LED Output

The drive provides an open-drain driver with 15mA of current sink capability to the Ready LED Output signal. The cathode of the LED should be connected to this signal. The LED and the current-limiting resistor must be provided by the enclosure.

6.2 Environment

6.2.1 Temperature and Humidity

Table 10   Temperature and Humidity

System Responsibility	
The system is responsible for maintaining a drive sensor temperature below 60C. Drive sensor temperature is as reported using SMART SCT.	
Operating ambient conditions	
Temperature Relative Humidity Maximum wet bulb temperature Maximum temperature gradient Maximum Relative Humidity gradient Altitude	5 to 60°C 5 to 90% non-condensing 29.4°C non-condensing 20°C/Hour 20%/Hr –300 to 3,048 m
Non-Operating conditions	
Temperature Relative humidity Maximum wet bulb temperature Maximum temperature gradient Maximum Relative Humidity gradient Altitude	-40 to 70°C 5 to 95% non-condensing 35°C non-condensing 20°C/Hour 20%/Hr –300 to 12,000 m (Inside dashed-dotted line of Figure 5)

Notes:
1. *Non-condensing conditions should be maintained at all times.*

Figure 5   Limits of Temperature and Altitude
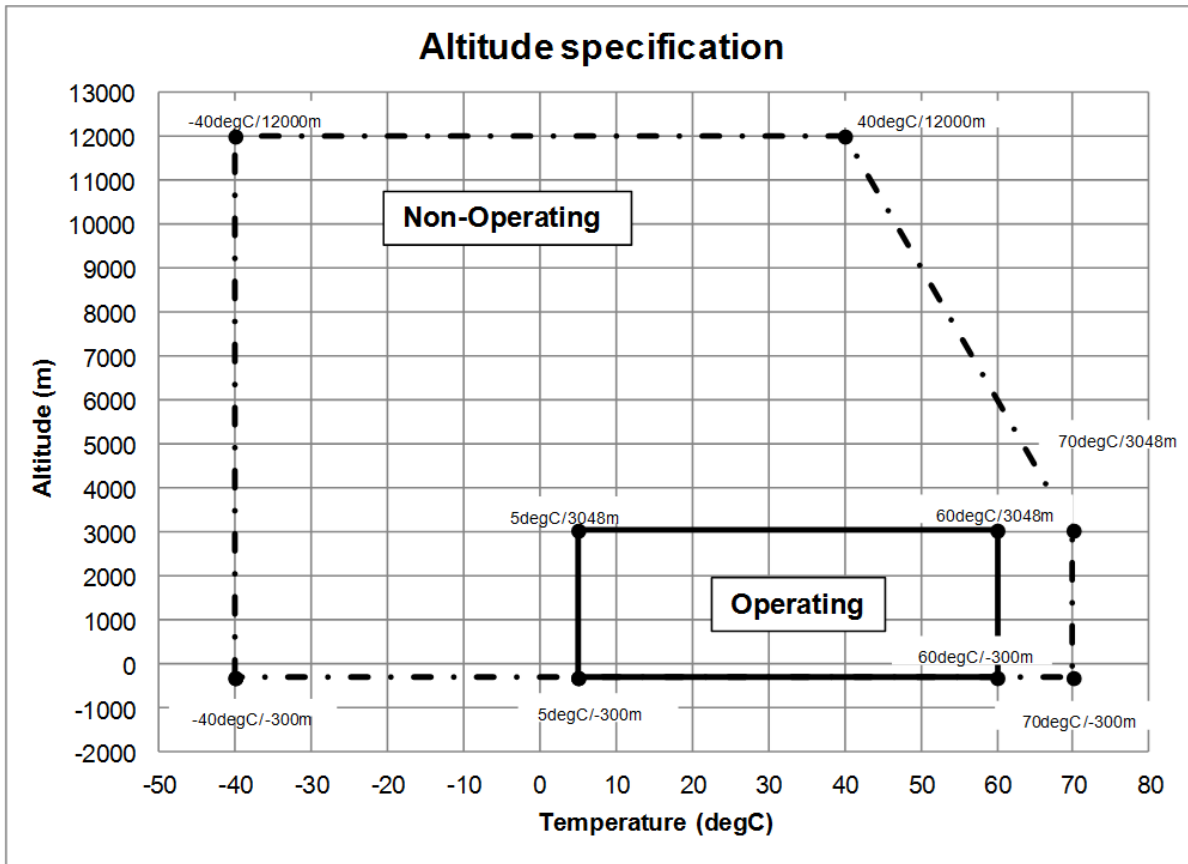
Figure 6   Limits of Temperature and Humidity
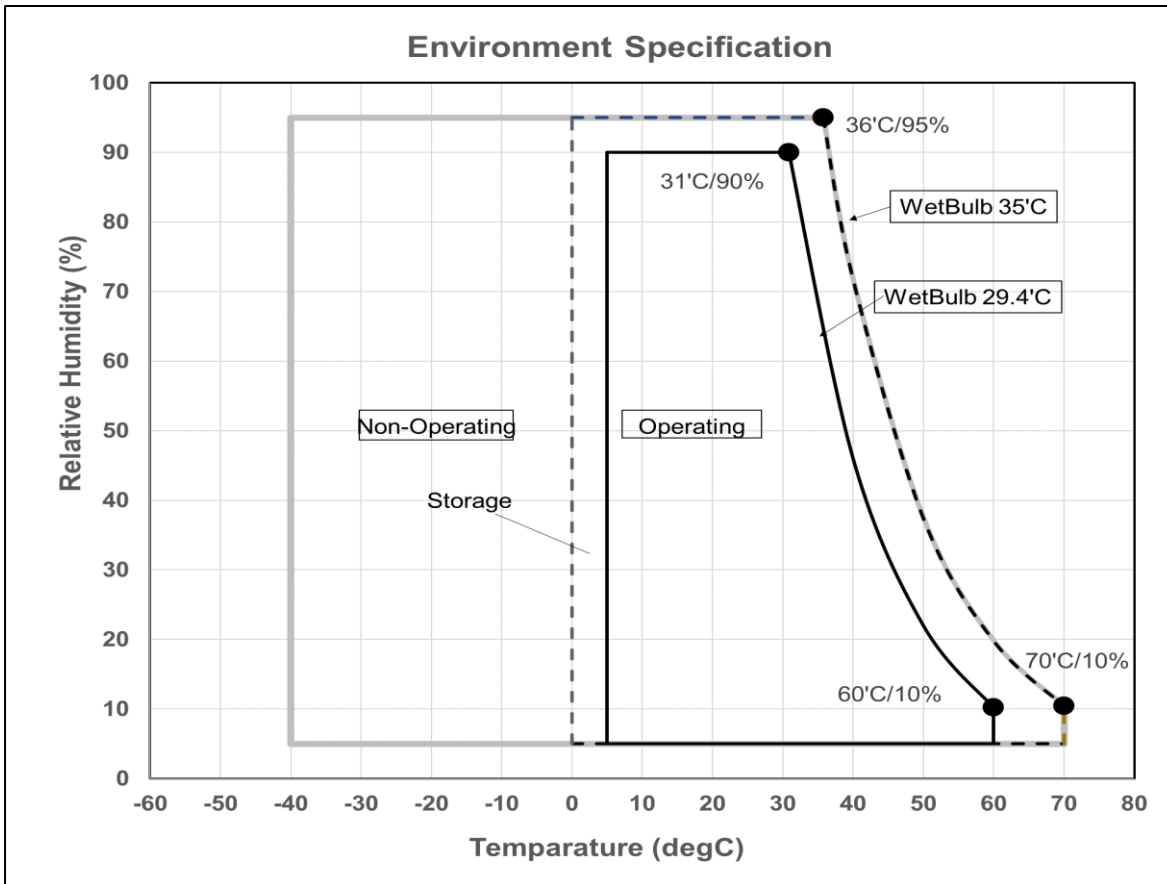
6.2.2   Storage Requirements

6.2.2.1   Packaging

The drive or option kit must be heat-sealed in a moisture barrier bag with bag supplied by Western Digital.

6.2.2.2   Storage

Maximum storage periods are 180 days within original, unopened Western Digital shipping bag or 60 days in an opened bag or outside the bag, while maintaining a temperature range of $0^{\circ}C$-$60^{\circ}C$ and the specified humidity and altitude limits in the Environmental section of this manual.

Storage can be extended to 1 year packaged or unpackaged under optimal environmental conditions (<25°C, <40% relative humidity non-condensing, and non-corrosive environment).

During any storage period, the drive shock, vibration, magnetic and electrical field specifications should be followed.

6.2.3   Atmospheric Condition

Environments that contain elevated levels of corrosives (e.g., hydrogen sulfide, sulfur oxides, or hydrochloric acid) should be avoided. Care must be taken to avoid using any compound/material in a way that creates an elevated level of corrosive materials in the atmosphere surrounding the disk drive. Care must also be taken to avoid use of any organometallic (e.g., organosilicon, or organotin) compound/material in a way that creates elevated vapor levels of these compounds/materials in the atmosphere surrounding the disk drive.

6.3   DC Power Requirements

Damage to the drive electronics may result if the power supply cable is connected or disconnected to the legacy Power connector while power is being applied to the drive (no hot plug/unplug is allowed). If SATA power supply cable is connected or disconnected to the SATA power connector, hot plug/unplug is allowed.

Table values for current and power are considered 'typical' values. Typical is defined as observed average or observed maximum in a sample of 6 drives per model under voltage conditions of 5.0V and 12.0V at the drive reported temperatures as noted.

6.3.1   Input Voltage

Table 11   Input Voltage

Input Voltage	During run and spin up	Absolute Max Spike Voltage	Supply Voltage Rise Time	Initial Capacitance
+5 Volts Supply	5V ± 5%	–0.3 to 5.5V	0 to 200ms	1 uF
+12 Volts Supply	12V ± 5%	–0.3 to 15.0V	0 to 400ms	1 uF

Caution: To avoid damage to the drive electronics, power supply voltage spikes must not exceed specifications.

6.3.2 Power Supply Current

6.3.2.1 SATA, 8TB, Block Size 512e, 6Gb/sec

Table 12 SATA Power Consumption, 8TB, 512e

8TB Model

(SATA) Serial ATA @ 6Gb/sec

	IO/Sec	+5V Current (Amp)	+12V Current (Amp)	Power (Watts)
Max Peak Operational [1]		1.32	2.04	
Start up Peak DC [2]		0.48	1.41	
Start up Peak AC [3]		0.78	2.10	
Idle_0 Ave.		0.32	0.41	6.5
Idle Ripple		0.07	0.04	
Random RW 50/50 8KB Qd=1 WCE=0 Peak @ 40IOPs [1]		1.21	2.02	
Random RW 50/50 8KB Qd=1 WCE=0 Ave. @ 40IOPs	40	0.33	0.51	7.7
Random RW 50/50 4KB Qd=4 WCE=0 Peak [1]		1.21	2.04	
Random RW 50/50 4KB Qd=4 WCE=0 Ave.	190	0.37	0.75	10.9
Random RW 70/30 4KB Qd=4 WCE=0 Peak [1]		1.21	2.04	
Random RW 70/30 4KB Qd=4 WCE=0 Ave.	153	0.37	0.81	11.5
Random RW 50/50 4KB Qd=1 WCE=0 Peak [1]		1.19	2.03	
Random RW 50/50 4KB Qd=1 WCE=0 Ave.	141	0.36	0.66	9.7
Max Power Workload				
Random Read 4KB Qd=16 Peak [1]		1.21	2.03	
Random Read 4KB Qd=16 Ave.	157	0.37	0.81	11.6
Sequential Read 64KB Qd=16 Peak [1]	MiB/s	1.09		
Sequential Read 64KB Qd=16 Ave. [4]	260	0.72	0.42	8.6
Sequential Write 64KB Qd=16 Peak [1]	MiB/s	0.73		
Sequential Write 64KB Qd=16 Ave. [4]	258	0.57	0.41	7.8

Power Save Mode	+5V Current (Amp)	+12V Current (Amp)	Power (Watts)	Power Saved (Watts) [5]
Idle_A	0.32	0.41	6.5	0.0
Idle_B	0.08	0.35	4.6	1.9
Idle_C	0.09	0.25	3.4	3.1
Standby_Y	0.09	0.25	3.4	3.1
Standby_Z	0.08	0.005	0.5	6.0
Sleep	0.08	0.005	0.5	6.0

PHY power condition	Port A Power Saved (Watts)
Partial	0.10
Slumber	0.27

Notes	6 HDDs per model
Sample size	
Temperature	HDD reported temperature = 40°C (25°C for Start up)
Sampling Rate	52.5K measurements/sec
PHY	Single port, 6Gb/s

[1]   Peak current is established via the average current in a 16 usec moving window. The peak values of the HDD in the population are then averaged and reported.

[2]   Start up DC (average) current is measured within a 200ms sliding window. The peak DC values of the HDD in the population are then averaged and reported.

[3]   Start up AC current is sampled at 62.5 kHz. The peak sample values of the HDD in the population are then averaged and reported.

[4]   Average measured at sustained sequential streaming rate

[5]   Power saved and compared to Idle_0

Table 13   SATA Power Consumption, 6TB, 512e

(SATA) Serial ATA @ 6Gb/sec   6TB model

	IO/Sec	+5V Current (Amp)	+12V Current (Amp)	Power (Watts)
Max Peak Operational [1]		1.31	1.96	
Start up Peak DC [2]		0.48	1.40	
Start up Peak AC [3]		0.77	2.05	
Idle_0 Ave.		0.32	0.33	5.5
Idle Ripple		0.06	0.08	
Random RW 50/50 8KB Qd=1 WCE=0 Peak @ 40IOPs [1]		1.16	1.93	
Random RW 50/50 8KB Qd=1 WCE=0 Ave. @ 40IOPs	40	0.33	0.43	6.8
Random RW 50/50 4KB Qd=4 WCE=0 Peak [1]		1.19	1.95	
Random RW 50/50 4KB Qd=4 WCE=0 Ave.	191	0.37	0.67	9.9
Random RW 70/30 4KB Qd=4 WCE=0 Peak [1]		1.20	1.95	
Random RW 70/30 4KB Qd=4 WCE=0 Ave.	153	0.37	0.73	10.5
Random RW 50/50 4KB Qd=1 WCE=0 Peak [1]		1.19	1.94	
Random RW 50/50 4KB Qd=1 WCE=0 Ave.	140	0.36	0.58	8.7
Max Power Workload				
Random Read 4KB Qd=32 Peak [1]		1.22	1.95	
Random Read 4KB Qd=32 Ave.	186	0.38	0.73	10.6
Sequential Read 64KB Qd=16 Peak [1]	MiB/s	1.06		
Sequential Read 64KB Qd=16 Ave. [4]	262	0.73	0.33	7.6
Sequential Write 64KB Qd=16 Peak [1]	MiB/s	0.71		
Sequential Write 64KB Qd=16 Ave. [4]	259	0.58	0.33	6.8

Power Save Mode	+5V Current (Amp)	+12V Current (Amp)	Power (Watts)	Power Saved (Watts) [5]
Idle_A	0.32	0.33	5.5	0.0
Idle_B	0.09	0.28	3.8	1.7
Idle_C	0.09	0.20	2.9	2.6
Standby_Y	0.09	0.20	2.9	2.6
Standby_Z	0.08	0.005	0.5	5.0
Sleep	0.08	0.005	0.5	5.0

PHY power condition	Port A Power Saved (Watts)
Partial	0.10
Slumber	0.27

Notes

Sample size	6 HDDs per model
Temperature	HDD reported temperature = 40°C (25°C for Start up)
Sampling Rate	52.5K measurements/sec
PHY	Single port, 6Gb/s

[1]   Peak current is established via the average current in a 16 usec moving window. The peak values of the HDD in the population are then averaged and reported.

[2]   Start up DC (average) current is measured within a 200ms sliding window. The peak DC values of the HDD in the population are then averaged and reported.

[3]   Start up AC current is sampled at 62.5 kHz. The peak sample values of the HDD in the population are then averaged and reported.

[4]   Average measured at sustained sequential streaming rate

[5]   Power saved and compared to Idle_0

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Table 14   SATA Power Consumption, 4TB, 512e

(SATA) Serial ATA @ 6Gb/sec   4TB model

	IO/Sec	+5V Current (Amp)	+12V Current (Amp)	Power (Watts)
Max Peak Operational [1]		1.25	1.96	
Start up Peak DC [2]		0.47	1.39	
Start up Peak AC [3]		0.77	2.02	
Idle_0 Ave.		0.32	0.32	5.4
Idle Ripple		0.05	0.07	
Random RW 50/50 8KB Qd=1 WCE=0 Peak @ 40IOPs [1]		1.01	1.93	
Random RW 50/50 8KB Qd=1 WCE=0 Ave. @ 40IOPs	40	0.33	0.42	6.7
Random RW 50/50 4KB Qd=4 WCE=0 Peak [1]		1.14	1.96	
Random RW 50/50 4KB Qd=4 WCE=0 Ave.	193	0.37	0.67	9.9
Random RW 70/30 4KB Qd=4 WCE=0 Peak [1]		1.17	1.96	
Random RW 70/30 4KB Qd=4 WCE=0 Ave.	155	0.37	0.72	10.5
Random RW 50/50 4KB Qd=1 WCE=0 Peak [1]		1.07	1.95	
Random RW 50/50 4KB Qd=1 WCE=0 Ave.	143	0.36	0.57	8.6
Max Power Workload				
Random Read 4KB Qd=16 Peak [1]		1.18	1.94	
Random Read 4KB Qd=16 Ave.	158	0.37	0.73	10.6
Sequential Read 64KB Qd=16 Peak [1]	MiB/s	0.93		
Sequential Read 64KB Qd=16 Ave. [4]	263	0.72	0.32	7.4
Sequential Write 64KB Qd=16 Peak [1]	MiB/s	0.71		
Sequential Write 64KB Qd=16 Ave. [4]	263	0.58	0.32	6.7

Power Save Mode	+5V Current (Amp)	+12V Current (Amp)	Power (Watts)	Power Saved (Watts) [5]
Idle_A	0.32	0.32	5.4	0.0
Idle_B	0.09	0.28	3.8	1.6
Idle_C	0.09	0.20	2.8	2.6
Standby_Y	0.09	0.20	2.8	2.6
Standby_Z	0.08	0.005	0.5	4.9
Sleep	0.08	0.005	0.5	4.9

PHY power condition	Port A Power Saved (Watts)
Partial	0.10
Slumber	0.27

Notes

Sample size	6 HDDs per model
Temperature	HDD reported temperature = 40°C (25°C for Start up)
Sampling Rate	52.5K measurements/sec
PHY	Single port, 6Gb/s

[1]   Peak current is established via the average current in a 16 usec moving window. The peak values of the HDD in the population are then averaged and reported.

[2]   Start up DC (average) current is measured within a 200ms sliding window. The peak DC values of the HDD in the population are then averaged and reported.

[3]   Start up AC current is sampled at 62.5 kHz. The peak sample values of the HDD in the population are then averaged and reported.

[4]   Average measured at sustained sequential streaming rate

[5]   Power saved and compared to Idle_0

6.3.3 Power Line Noise Limits

Table 15 Allowable Power Supply Noise Limits at Drive Power Connector

	Noise Voltage (mV pp)	Frequency Range
+5V DC	250	100Hz-20MHz
+12V DC	800	100Hz-8KHz
	450	8KHz-100KHz
	250	100KHz-20MHz

During drive operation, both 5 and 12-volt ripple are generated by the drive due to dynamic loading of the power supply. This voltage ripple will add to existing power supply voltage ripple. The sum is the power line noise.

To prevent significant performance loss, the power line noise level when measured at the drive power connector should be kept below the limits in the above table.

6.3.4 Power Consumption Efficiency

Table 16 Power Consumption Efficiency

Power Consumption Efficiency at Idle	SATA
W/TB	0.813 (8TB), 0.917 (6TB), 1.35 (4TB)

6.4 Reliability

6.4.1 Annualized Failure Rate

This product has a projected 0.44% AFR specification rating based on typical workload and temperatures.
The AFR specification is based on a sample population and is estimated by statistical measurements and acceleration algorithms under typical operating conditions at 40C device reported temperature.
Derating of AFR will occur above these parameters, up to 550TB/YR workload and 60C (device reported temp).
AFR ratings do not predict an individual drive's reliability and do not constitute a warranty.

6.4.2 Data Integrity

When the write cache option is disabled, no customer data is lost during power loss. If the write cache option is active or has been recently used, some data loss can occur during power loss.   To prevent the loss of data at power off, confirm the successful completion of a FLUSH CACHE (E7h) or FLUSH CACHE EXT (EAh) command.

6.4.3 Cable Noise Interference

To avoid any degradation of performance throughput or error rate when the interface cable is routed on top or comes in contact with the HDA assembly, the drive must be grounded electrically to the system frame by four screws. The common mode noise or voltage level difference between the system frame and power cable ground or AT interface cable ground should be in the allowable level specified in the power requirement section.

6.4.4 Load/Unload

The product supports a minimum of 600,000 normal load/unloads in a 40° C environment.
Load/unload is invoked by transition of the HDD's power mode. (Chapter 4.5.3 Operating Modes)
    Idle (Idle_A) <-> unload idle (Idle_B)
    Idle (Idle_A) <-> Low rpm idle (Idle_C)

6.4.5   Start/Stop Cycles

The drive withstands a minimum of 50,000 start/stop cycles in a 40° C environment and a minimum of 10,000 start/stop cycles in extreme temperature or humidity within the operating range.

6.4.6   Preventive Maintenance

None

6.4.7   Data Reliability

Probability of not recovering data is 1 in 10^{15} bits read.

LDPC on-the-fly/ offline data correction

- 4608 bit LDPC
- This implementation recovers maximum 2500 bits single burst error by on the fly correction and maximum 3500 bits single burst error by offline correction.

6.4.8   Workload

The maximum rated workload is <550TB/YR. The workload can be comprised of reads and/or writes.
The maximum rated workload is specified for operating at typical temperatures.
Occasional* excursions in operating conditions between the "typical AFR specification conditions" and the "maximum drive operating conditions" may occur without significant impact to reliability.

*Occasional excursions shall not exceed 2% of total run time.

6.4.9   Required Power-Off Sequence

The required sequence for removing power from the drive is as follows:

Step 1: Issue a STOP UNIT Command
        Standby
        Standby immediate
        Sleep
Note: Do not use the Flush Cache command for the power off sequence because this command does not invoke Unload

Step 2: Wait until the Command Complete status is returned. However, the time out value needs to be 60 seconds considering error recovery time.

Step 3: Terminate power to HDD.

6.5   Mechanical Specifications

6.5.1   Physical Dimensions

The following table shows the physical dimensions of the drive.

Table 17   Physical Dimensions

Height (mm)	Width (mm)	Length (mm)	Weight (grams)
26.1 Max	101.6 ± 0.25	147 Max	715 Max

6.5.1.1   SATA

Figure 7   Top, bottom, side views and mechanical dimensions, with connector position (SATA)
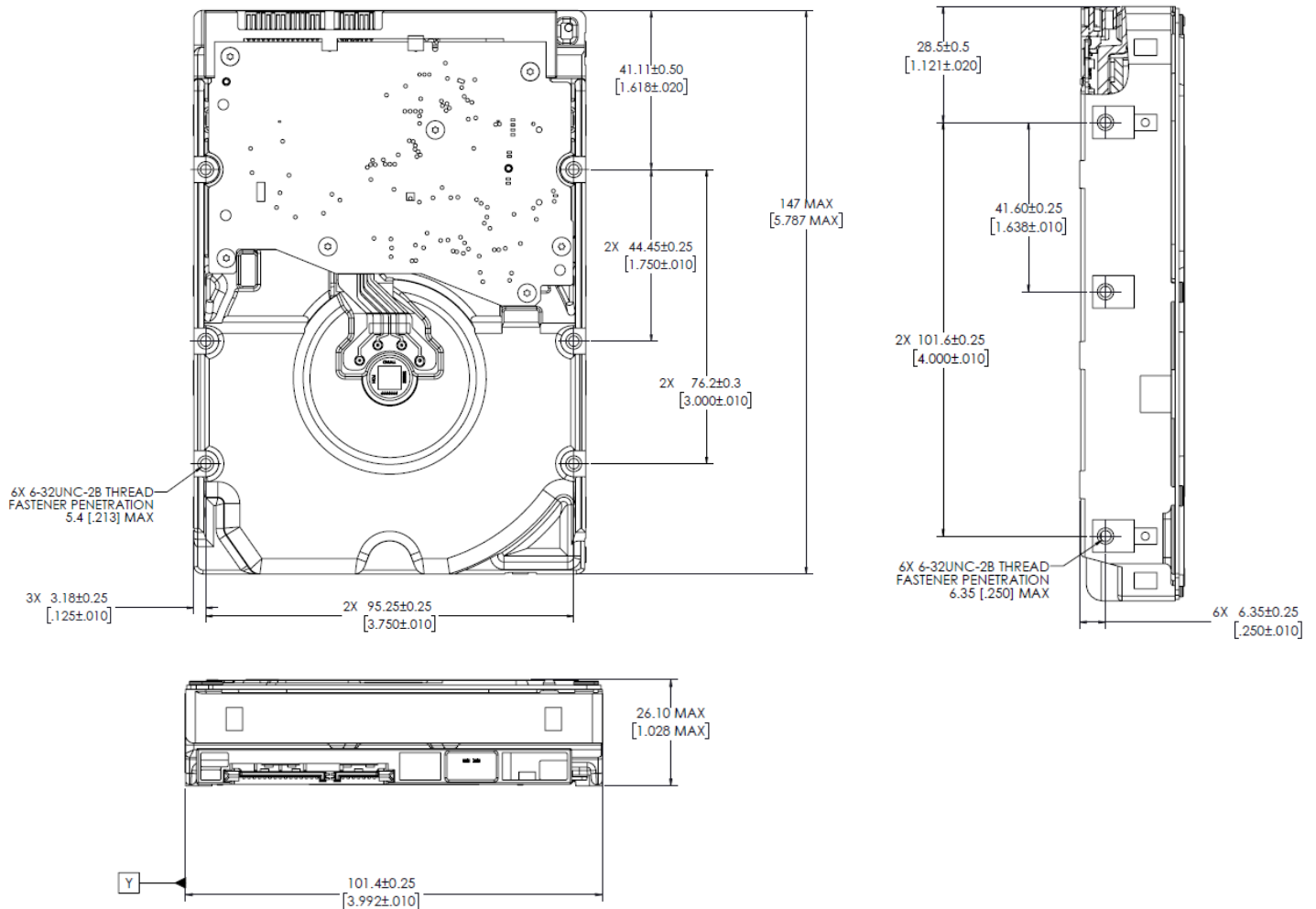
All dimensions are in millimeters.
(numbers in brackets are in inchess)

6.5.2   Drive Mounting

The drive will operate in all axes (6 directions). Performance and error rate will stay within specification limits if the drive is operated in other orientations than that in which it was formatted.

For reliable operation, the drive must be mounted in the system securely enough to prevent excessive motion or vibration of the drive during seek operation or spindle rotation, using appropriate screws or equivalent mounting hardware.

The recommended mounting screw torque is 0.6 - 1.0 Nm (6-10 Kgf.cm).

The recommended mounting screw depth is 3.8 mm maximum for bottom and 6.1 mm maximum for horizontal mounting.

Drive level vibration test and shock test are to be conducted with the drive mounted to the table using the bottom four screws.

6.5.3   Heads Unload and Actuator Lock

Heads are moved out from disks (unload) to protect the disk data during shipping, moving, or storage.   Upon power down, the heads are automatically unloaded from disk area and the locking mechanism of the head actuator will secure the heads in unload position.

6.6   Vibration and Shock

All vibration and shock measurements recorded in this section are made with a drive that has no mounting attachments for the systems. The input power for the measurements is applied to the normal drive mounting points.

6.6.1   Operating Vibration

6.6.1.1   Random Vibration Linear

The test is 30 minutes of random vibration using the power spectral density (PSD) levels shown below in each of three mutually perpendicular axes. The disk drive will operate without non-recoverable errors when subjected to the below random vibration levels.

Table 18   Random Vibration PSD Profile Break Points (operating)

Frequency	5 Hz	17 Hz	45 Hz	48 Hz	62 Hz	65 Hz	150 Hz	200 Hz	500 Hz	RMS (m/sec^2)
$[(m/sec^2)^2/Hz]$	1.9 x 10E–3	1.1 x 10E–1	1.1 x 10E–1	7.7 x 10E–1	7.7 x 10E–1	9.6 x 10E–2	9.6 x 10E–2	4.8 x 10E–2	4.8 x 10E-2	6.57

The overall RMS (Root Mean Square) level is 6.57 m/sec^2 (0.67 G).

6.6.1.2   Swept Sine Vibration (Linear)

The drive will meet the criteria shown below while operating in the specified conditions:

- No errors occur with 4.9 m/sec^2 (0.5 G) 0 to peak, 5 to 300 to 5 Hz sine wave, 0.5 oct/min sweep rate with 3- minute dwells at two major resonances
- No data loss occurs with 9.8 m/sec^2 (1 G) 0 to peak, 5 to 300 to 5 Hz sine wave, 0.5 oct/min sweep rate with 3- minute dwells at two major resonances

6.6.1.3   Random Vibration (Rotational)

The drive will meet the criteria shown below while operating in the specified conditions:

- Less than 20% performance degradation
- The overall RMS (Root Mean Square) level of vibration is 12.5 Rad/sec^2. PSD profile is shown below.

Table 19   Random Vibration (Rotational) PSD Profile Break Points

Frequency	20 Hz	100 Hz	200 Hz	800 Hz	1000 Hz	1500 Hz	1700 Hz	2000 Hz	RMS (Rad/s^2)
$[(Rad/s^2)^2/Hz]$	1.90 x 10E–2	1.90 x 10E–2	1.87 x 10E–1	1.87 x 10E–1	5.33 x 10E–2	7.70 x 10E–3	4.00 x 10E-03	4.00 x 10E-03	12.5

6.6.2 Nonoperating Vibration

The drive does not sustain permanent damage or loss of previously recorded data after being subjected to the environment described below

6.6.2.1 Random Vibration

The test consists of a random vibration applied for each of three mutually perpendicular axes with the time duration of 10 minutes per axis. The PSD levels for the test simulate the shipping and relocation environment shown below. The overall RMS (Root Mean Square) level of vibration is 10.2 m/sec^2 (1.04 G).

Table 20   Random Vibration PSD Profile Break Points (nonoperating)

Frequency	2 Hz	4 Hz	8 Hz	40 Hz	55 Hz	70 Hz	200 Hz
[(m/sec^2)^2/Hz]	0.096	2.89	2.89	0.289	0.962	0.962	0.096

6.6.2.2 Swept Sine Vibration

- 19.6 m/sec^2 (2 G) (Zero to peak), 5 to 500 to 5 Hz sine wave
- 0.5 oct/min sweep rate
- 3 minutes dwell at two major resonances

6.6.3 Operating Shock

The drive meets the following criteria while operating in the conditions described below. The shock test consists of 10 shock inputs in each axis and direction for total of 60. There must be a delay between shock pulses long enough to allow the drive to complete all necessary error recovery procedures.

- No hard error occurs with a 98.1 m/sec^2 (10 G) half-sine shock pulse of 11 ms duration
- No hard error occurs with a 294 m/sec^2 (30 G) half-sine shock pulse of 4 ms duration
- No hard error occurs with a 686 m/sec^2 (70 G, Write/Read), half-sine shock pulse of 2 ms duration

6.6.4 Nonoperating Shock

The drive will operate without non-recoverable errors after being subjected to shock pulses with the following characteristics.

6.6.4.1 Trapezoidal Shock Wave

- Approximate square (trapezoidal) pulse shape
- Approximate rise and fall time of pulse is 1 ms
- Average acceleration level is 490 m/sec^2 (50 G). (Average response curve value during the time following the 1 ms rise time and before the 1 ms fall with a time "duration of 11 ms")
- Minimum velocity change is 4.23 m/sec

6.6.4.2   Sinusoidal Shock Wave

The shape is approximately half-sine pulse. The table below shows the maximum acceleration level and duration.

Table 21   Sinusoidal Shock Wave

Acceleration Level (m/sec^2) (G)	Duration (ms)
2940 (300G)	2
1470 (150G)	11

6.6.5   Nonoperating Rotational Shock

All shock inputs shall be applied around the actuator pivot axis.

Table 22   Rotational Shock

Duration	Rad/sec^2
1 ms	30,000
2 ms	20,000

6.7   Acoustics

The upper limit criteria of the octave sound power levels are given in Bels relative to one picowatt and are shown in the following table. The sound power emission levels are measured in accordance with ISO 7779.

Table 23   Sound Power Levels

Mode	7200 rpm (Typical / Max, Bels)
Idle	2.9
Operating	3.6

Mode definition:

Idle mode   The drive is powered on, disks spinning, track following, unit ready to receive and respond to interface commands.

Operating mode   Continuous random cylinder selection and seek operation of the actuator with a dwell time at each cylinder. The seek rate for the drive is to be calculated as shown below:

- Dwell time = 0.5 x 60/RPM
- Seek rate = 0.4 / (Average seek time + Dwell time)

6.8   Identification Labels

The following labels are affixed to every drive shipped from the drive manufacturing location in accordance with the appropriate hard disk drive assembly drawing:

- A label containing the Western Digital logo and the part number
- A label containing the drive model number, the manufacturing date code, the formatted capacity, the place of manufacture, certification logos from various safety agencies (e.g. UL/CSA/CE/RCM, etc.)
- A bar code label containing the drive serial number
- A label containing the jumper pin description
- A user designed label per agreement
- The above labels may be integrated with other labels.

6.9   Safety

6.9.1   UL and CSA Standard Conformity

The product is qualified per UL 62368-1, 3rd Edition and CAN/CSA No.62368-1-14 3rd Edition for Audio/video, information and communication technology equipment Part 1: Safety requirements.

The UL recognition or the CSA certification is maintained for the product life

The UL and C-UL certification mark is on the drive.

6.9.2   EU Safety Standard Conformity

The product is approved by TUV complying EN 62368-1 : 2020+A1 standard.

6.9.3   Flammability

The printed circuit boards used in this product are made of material with the UL recognized flammability rating of V-1 or better. The flammability rating is marked or etched on the board. All other parts not considered electrical components are made of material with the UL recognized flammability rating of V-2 minimum.

6.9.4   Safe Handling

The product is conditioned for safe handling in regards to sharp edges and corners.

6.9.5   Substance Restriction Requirements

he product complies with the Directive 2011/65/EU and Directive (EU) 2015/863 on the restriction of the use of certain hazardous substances in electrical and electronic equipment (RoHS),
the Substances of Very High Concern (SVHC) updated candidates of European Union Regulation 1907/2006 on the Registration Evaluation Authorization and Restriction of Chemicals (REACH),
China RoHS Directive, Taiwan BSMI and with Halogen free requirements based on the electronics industry standard, IEC 61249-2-21 (*http://www.iec.ch/*).

6.9.6   Secondary Circuit Protection

The product contains both 5V and 12V over-current protection circuitry.

6.10   Electromagnetic Compatibility

When installed in a suitable enclosure and exercised with a random accessing routine at maximum data rate, the drive meets the following worldwide EMC requirements:

- United States Federal Communications Commission (FCC) Code of Federal Regulations, Part 15 (Class B)
- EN 55032: Electromagnetic compatibility of multimedia equipment - Emission Requirements
- EN 55035: Electromagnetic compatibility of multimedia equipment - Immunity requirements

6.10.1   CE Mark

The product is declared to be in conformity with requirements of the following EC directives.

EMC Directive 2014/30/EU on electromagnetic compatibility.

RoHS Directive 2011/65/EU and (EU) 2015/863 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

6.10.2   RCM Mark

The product complies with the standard of Electromagnetic compatibility of multimedia equipment – Emission requirements, EN 55032, which is required by Australian Communications and Media Authority.

6.10.3   BSMI Mark

The product complies with the Taiwan's EMC standard of information technology equipment – Radio disturbance characteristics – Limits and methods of measurement, CNS 13438 Class B.

6.10.4.   KC Mark

The product complies with the Korean EMC standards of KS C 9832:2019 for Emission and KS C 9835:2019 for Immunity. The product is registered under Broadcasting and Communication Equipment.

6.11   Third Party Open-Source Licenses

This product may include or use the following open source software subject to the following open source licenses. If required by the applicable open source license, Western Digital may provide the open source code to you on request either electronically or on a physical storage medium for a charge covering the cost of performing such distribution, which may include the cost of media, shipping, and handling.
Each third-party component that may be included is listed below, followed by its associated license text.

Components:

LZHUF 4/7/1989 : LZHUF
A portable, fast, and free implementation of the MD5 Message-Digest Algorithm (RFC 1321) 1.10 : Peslyak Public Domain with fallback

Licenses:

LZHUF
(LZHUF 4/7/1989)

LZHUF.C (c)1989 by Haruyasu Yoshizaki, Haruhiko Okumura, and Kenji Rikitake.
All rights reserved. Permission granted for non-commercial use.

Peslyak Public Domain with fallback
(A portable, fast, and free implementation of the MD5 Message-Digest Algorithm (RFC 1321) 1.10)

 * This is an OpenSSL-compatible implementation of the RSA Data Security, Inc.
 * MD5 Message-Digest Algorithm (RFC 1321).

 * Homepage:
 * http://openwall.info/wiki/people/solar/software/public-domain-source-code/md5

 * Author:
 * Alexander Peslyak, better known as Solar Designer <solar at openwall.com>

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 * general public under the following terms:

* Redistribution and use in source and binary forms, with or without
* modification, are permitted.

* There's ABSOLUTELY NO WARRANTY, express or implied.

* (This is a heavily cut-down "BSD license".)

* This differs from Colin Plumb's older public domain implementation in that
* no exactly 32-bit integer data type is required (any 32-bit or wider
* unsigned integer data type will do), there's no compile-time endianness
* configuration, and the function prototypes match OpenSSL's. No code from
* Colin Plumb's implementation has been reused; this comment merely compares
* the properties of the two independent implementations.

* The primary goals of this implementation are portability and ease of use.
* It is meant to be fast, but not as fast as possible. Some known
* optimizations are not included to reduce source code size and avoid
* compile-time configuration.

Part 2. Interface Specification

7 General

7.1 Introduction

This specification describes the host interface of WUS72120xBLE6xx.

The interface conforms to the following working documents of Information technology with certain limitations described in *Section 7.3 "Deviations from Standard".*

- *S*erial ATA International Organization: Serial ATA Revision 3.5

7.2 Terminology

Device   Device indicates WUS72120xBLE6xx.

Host   Host indicates the system that the device is attached to.

7.3 Deviations From Standard

The device conforms to the referenced specifications, with deviations described below.

Check Power Mode	If the Extended Power Conditions feature set is disabled and the device is in Idle mode, Check Power Mode command returns FFh by Sector Count Register, instead of returning 80h. Refer to *Section 11.1 "Check Power Mode"* for detail.
COMRESET	COMRESET response is not the same as that of Power On Reset. Refer to *Section 9.1 "Reset Response"* for detail..
Download	Both Download Microcode and Download Microcode DMA are aborted when the device is in security locked mode.
COMRESET response time	During 500ms from Power On Reset, COMINIT is not returned within 10ms as a response to COMRESET.
SCT Error Recovery Control	When the device is in standby mode, any command where error recovery time limit is specified can't be completed while waiting for the spindle to reach operating speed even if execution time exceeds specified recovery time limit. The minimum time limit is 6.5 second. When the specified time limit is shorter than 6.5 second, the issued command is aborted.

8 Registers

In Serial ATA, the host adapter contains a set of registers that shadow the contents of the traditional device registers, referred to as the Shadow Register Block. Shadow Register Block registers are interface registers used for delivering commands to the device or posting status from the device. About details, please refer to the Serial ATA Specification.

In the following cases, the host adapter sets the BSY bit in its shadow Status Register and transmits a FIS to the device containing the new contents.

- Command register is written in the Shadow Register Block
- Device Control register is written in the Shadow Register Block with a change of state of the SRST bit
- COMRESET is requested

8.1 Alternate Status Register

Table 24   Alternate Status Register

Alternate Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC /SERV	DRQ	COR	IDX	ERR

This register contains the same information as the Status Register. The only difference is that reading this register does not imply interrupt acknowledge or clear a pending interrupt. See *Section 8.11 "Status Register"* for the definition of the bits in this register.

8.2 Command Register

This register contains the command code being sent to the device. Command execution begins immediately after this register is written. The command set is shown in *Section 11 "Command Descriptions"*.

All other registers required for the command must be set up before writing the Command Register.

8.3 Cylinder High Register

This register contains the high order bits of the starting cylinder address for any disk access. At the end of the command, this register is updated to reflect the current cylinder number.

In LBA Mode this register contains Bits 16-23. At the end of the command, this register is updated to reflect the current LBA Bits 16-23.

The cylinder number may be from zero to the number of cylinders minus one.

When 48-bit addressing commands are used, the "most recently written" content contains LBA Bits 16-23, and the "previous content" contains Bits 40-47. The 48-bit Address feature set is described in *Section 9.12 "48-bit Address Feature Set" 9.12*.

8.4   Cylinder Low Register

This register contains the low order bits of the starting cylinder address for any disk access. At the end of the command, this register is updated to reflect the current cylinder number.

In LBA Mode this register contains Bits 8-15. At the end of the command, this register is updated to reflect the current LBA Bits 8-15.

The cylinder number may be from zero to the number of cylinders minus one.

When 48-bit addressing commands are used, the "most recently written" content contains LBA Bits 8-15, and the "previous content" contains Bits 32-39.

8.5   Device Control Register

Table 25   Device Control Register

Device Control Register							
7	6	5	4	3	2	1	0
HOB	-	-	-	1	SRST	-IEN	0

Bit Definitions

HOB   HOB (high order byte) is defined by the 48-bit Address feature set. A write to any Command Register shall clear the HOB bit to zero.

SRST (RST)   Software Reset. The device is held reset when RST=1. Setting RST=0 re-enables the device. The host must set RST=1 and wait for at least 5 microseconds before setting RST=0, to ensure that the device recognizes the reset.

-IEN   Interrupt Enable. When –IEN=0, and the device is selected, device interrupts to the host will be enabled. When –IEN=1, or the device is not selected, device interrupts to the host will be disabled.

8.6   Device/Head Register

Table 26   Device/Head Register

Device/Head Register							
7	6	5	4	3	2	1	0
1	L	1	DRV	HS3	HS2	HS1	HS0

This register contains the device and head numbers.

Bit Definitions

L   Binary encoded address mode select. When L=0, addressing is by CHS mode. When L=1, addressing is by LBA mode.

DRV   Device. This product ignores this bit.

HS3,HS2,HS1,HS0   Head Select. These four bits indicate binary encoded address of the head. HS0 is the least significant bit. At command completion, these bits are updated to reflect the currently selected head.

The head number may be from zero to the number of heads minus one.

In LBA mode, HS3 through HS0 contain bits 24-27 of the LBA. At command completion, these bits are updated to reflect the current LBA bits 24-27.

8.7   Error Register

Table 27   Error Register

Error Register							
7	6	5	4	3	2	1	0
ICRCE	UNC	0	IDNF	0	ABRT	TK0NF	AMNF

This register contains status from the last command executed by the device, or a diagnostic code.

At the completion of any command except Execute Device Diagnostic, the contents of this register are valid always even if ERR=0 in the Status Register.

Following a power on, a reset, or completion of an Execute Device Diagnostic command, this register contains a diagnostic code. *See Section 9.2 Diagnostic and Reset Considerations* for the definition.

Bit Definitions

ICRCE (CRC)   Interface CRC Error. ICRCE=1 indicates a CRC error occurred during FIS transmission or FIS reception.

UNC   Uncorrectable Data Error. UNC=1 indicates an uncorrectable data error has been encountered.

IDNF (IDN)   ID Not Found. IDN=1 indicates the requested sector's ID field could not be found.

ABRT (ABT)   Aborted Command. ABT=1 indicates the requested command has been aborted due to a device status error or an invalid parameter in an output register.

TK0NF (T0N)   Track 0 Not Found. T0N=1 indicates track 0 was not found during a Recalibrate command.

AMNF (AMN)   Address Mark Not Found. This product does not report this error. This bit is always zero.

8.8   Features Register

This register is command specific. This is used with the Set Features command, SMART Function Set command, and Sanitize Device Feature Set command.

8.9   Sector Count Register

This register contains the number of sectors of data requested to be transferred on a read or write operation between the host and the device. If the value in the register is set to 0, a count of 256 sectors (in 28-bit addressing) or 65,536 sectors (in 48-bit addressing) is specified.

If the register is zero at command completion, the command was successful. If not successfully completed, the register contains the number of sectors which need to be transferred in order to complete the request.

The contents of the register are defined otherwise on some commands. These definitions are given in the command descriptions.

8.10   Sector Number Register

This register contains the starting sector number for any disk data access for the subsequent command.
The sector number is from one to the maximum number of sectors per track.

In LBA mode, this register contains Bits 0-7. At the end of the command, this register is updated to reflect the current LBA Bits 0-7.

When 48-bit commands are used, the "most recently written" content contains LBA Bits 0-7, and the "previous content" contains Bits 24-31.

8.11   Status Register

Table 28   Status Register

Status Register							
7	6	5	4	3	2	1	0
BSY	DRDY	DF	DSC /SERV	DRQ	CORR	IDX	ERR

This register contains the device status. The contents of this register are updated whenever an error occurs and at the completion of each command.

If the host reads this register when an interrupt is pending, it is considered to be the interrupt acknowledge. Any pending interrupt is cleared whenever this register is read.

If BSY=1, no other bits in the register are valid.

Bit Definitions

BSY	Busy. BSY=1 whenever the device is accessing the registers. The host should not read or write any registers when BSY=1. If the host reads any register when BSY=1, the contents of the Status Register will be returned.
DRDY (RDY)	Device Ready. RDY=1 indicates that the device is capable of responding to a command. RDY will be set to 0 during power on until the device is ready to accept a command. If the device detects an error while processing a command, RDY is set to 0 until the Status Register is read by the host, at which time RDY is set back to 1.
DF	Device Fault. This product does not support DF bit. DF bit is always zero.
DSC	Device Seek Complete. DSC=1 indicates that a seek has completed and the device head is settled over a track. DSC is set to 0 by the device just before a seek begins. When an error occurs, this bit is not changed until the Status Register is read by the host, at which time the bit again indicates the current seek complete status.
	When the device enters into or is in Standby mode or Sleep mode, this bit is set by device in spite of not spinning up.
SERV (SRV)	Service. This product does not support SERV bit.
DRQ	Data Request. DRQ=1 indicates that the device is ready to transfer a word or byte of data between the host and the device. The host should not write the Command register when DRQ=1.
CORR (COR)	Corrected Data. Always 0.
IDX	Index. IDX=1 once per revolution. Since IDX=1 only for a very short time during each revolution, the host may not see it set to 1 even if the host is reading the Status Register continuously. Therefore, the host should not attempt to use IDX for timing purposes.
ERR	Error. ERR=1 indicates that an error occurred during execution of the previous command. The Error Register should be read to determine the error type. The device sets ERR=0 when the next command is received from the host.

9   General Operation Descriptions

9.1   Reset Response

There are three types of reset in ATA as follows:

Power On Reset (POR)   The device executes a series of electrical circuitry diagnostics.

COMRESET   COMRESET is issued in Serial ATA bus.
The device resets the interface circuitry as well as Soft Reset.

Soft Reset (Software Reset)   SRST bit in the Device Control Register is set, and then is reset.
The device resets the interface circuitry according to the Set Features requirement.

The actions of each reset are shown in the
following Table:

Table 29   Reset Response

	POR	COMRESET	Soft Reset
Aborting Host interface	-	o	o
Aborting Device operation	-	(*1)	(*1)
Initialization of hardware	o	x	x
Internal diagnostic	o	x	x
Spinning spindle	(*6)	x	x
Initialization of registers (*2)	o	o	o

Reverting programmed parameters to default
   - Number of CHS
  (set by Initialize Device Parameter)
   - Multiple mode
   - Write cache
   - Read look-ahead
   - ECC bytes
	o	(*3)	(*3)

Disable Standby timer	o	x	x
Power mode	(*5)	(*4)	(*4)

o----------Execute
x--------- Not execute

Table Notes

(*1)   Execute after the data in write cache has been written.

(*2)   Default value on POR is shown in this Table, and Default Register Values in *Section 9.1.1 "Register Initialization"*.

(*3)   The Set Features command with Feature register = CCh enables the device to revert these parameters to the power on defaults.

(*4)   In the case of Sleep mode, the device goes to Standby mode. In other case, the device does not change current mode.

(*5)   Idle when Power-Up in Standby feature set is disabled. Standby when Power-Up in Standby feature set is enabled.

(*6)   Spinning up when Power-Up in Standby feature set is disabled. Standby when Power-Up in Standby feature set is enabled.

9.1.1   Register Initialization

Table 30   Default Register Values

Register	Default Value
Error	Diagnostic Code
Sector Count	01h
Sector Number	01h
Cylinder Low	00h
Cylinder High	00h
Device/Head	00h
Status	50h
Alternate Status	50h

After power on, hard reset, or software reset, the register values are initialized as shown in this Table.

Table 31   Diagnostic Codes

Code	Description
01h	No error Detected
02h	Formatter device error
03h	Sector buffer error
04h	ECC circuitry error
05h	Controller microprocessor error

The meaning of the Error Register diagnostic codes resulting from power on, hard reset or the Execute Device Diagnostic command is shown in this Table.

9.2   Diagnostic and Reset Considerations

In each case of Power on Reset, COMRESET, Soft reset, and EXECUTE DEVICE DIAGNOSTIC command, the device is diagnosed. An Error register is set as shown in Table 30 above.

9.3   Sector Addressing Mode

All addressing of data sectors recorded on the device's media is by a logical sector address. The logical CHS address for HUS728T8TALx6xx is different from the actual physical CHS location of the data sector on the disk media. All addressing of data sectors recorded on the device's media.

HUS728T8TALx6xx support both Logical CHS Addressing Mode and LBA Addressing Mode as the sector addressing mode.

The host system may select either the currently selected CHS translation addressing or LBA addressing on a command-by-command basis by using the L bit in the DEVICE/HEAD register. So a host system must set the L bit to 1 if the host uses LBA Addressing mode.

9.3.1   Logical CHS Addressing Mode

The logical CHS addressing is made up of three fields: the cylinder number, the head number and the sector number. Sectors are numbered from 1 to the maximum value allowed by the current CHS translation mode but cannot exceed 255(0FFh). Heads are numbered from 0 to the maximum value allowed by the current CHS translation mode but cannot exceed 15(0Fh). Cylinders are numbered from 0 to the maximum value allowed by the current CHS translation mode but cannot exceed 65535(0FFFFh).

When the host selects a CHS translation mode using the INITIALIZE DEVICE PARAMETERS command, the host requests the number of sectors per logical track and the number of heads per logical cylinder. The device then computes the number of logical cylinders available in requested mode.

The default CHS translation mode is described in the Identify Device Information. The current CHS translation mode also is described in the Identify Device Information.

9.3.2 LBA Addressing Mode

Logical sectors on the device shall be linearly mapped with the first LBA addressed sector (sector 0) being the same sector as the first logical CHS addressed sector (cylinder 0, head 0, sector 1). Irrespective of the logical CHS translation mode currently in effect, the LBA address of a given logical sector does not change. The following is always true:

LBA = ((cylinder * heads_per_cylinder + heads)

                 * sectors_per_track) + sector - 1

Where heads_per_cylinder and sectors_per_track are the current translation mode values.

On LBA addressing mode, the LBA value is set to the following register.

Device/Head	←	LBA bits	27-24
Cylinder High	←	LBA bits	23-16
Cylinder Low	←	LBA bits	15- 8
Sector Number	←	LBA bits	7- 0

9.4 Power Management Feature Set

The power management feature set allows an application client to modify the behavior of a device in a manner that reduces the power required to operate. The power management feature set provides a set of commands and a timer that enables a device to implement low power consumption modes.

The Power Management feature set implements the following set of functions per ACS-4:

1. A Standby timer
2. Idle command
3. Idle Immediate command
4. Sleep command
5. Standby command
6. Standby Immediate command

9.4.1 Power Mode

The lowest power consumption when the device is powered on occurs in Sleep Mode. When in sleep mode, the device requires a reset to be activated.

In Idle Mode the device is capable of responding immediately to media access requests.

In Active Mode the device is under executing a command or accessing the disk media with read look-ahead function or writes cache function.

9.4.1.1 Active Idle Mode

Servo is mostly off, but heads are loaded. The spindle is rotated at the full speed.

9.4.1.2 Low Power Idle Mode

Additional electronics are powered off, and heads are unloaded on the ramp, however the spindle is still rotated at the full speed.

9.4.1.3 Low RPM Idle Mode

The heads are unloaded on the ramp, and the spindle is rotated at the 85-90% of the full speed.

9.4.1.4 Standby Mode

The device interface is capable of accepting commands, but as the media may not immediately accessible, there is a delay while waiting for the spindle to reach operating speed.

9.4.2   Power Management Commands

The Check Power Mode command allows a host to determine if a device is in, going, to or leaving standby or idle mode.

The Idle and Idle Immediate commands move a device to idle mode immediately from the active or standby modes. The idle command also sets the standby timer count and enables or disables the standby timer.

The Standby and Standby Immediate commands move a device to standby mode immediately from the active or idle modes. The standby command also sets the standby timer count and enables or disables the Standby timer

The Sleep command moves a device to Sleep mode. The device's interface becomes inactive after the device reports command completion for the Sleep command. A device only transitions from Sleep mode after processing a hardware reset or a software reset.

9.4.3   Standby Timer

The standby timer provides a method for the device to automatically enter standby mode from either active or idle mode following a host programmed period of inactivity. If the device is in the active or idle mode, the device waits for the specified time period and if no command is received, the device automatically enters the standby mode.

If the value of SECTOR COUNT Register on Idle command or Standby command is set to 00h, the standby timer is disabled.

9.4.4   Interface Capability for Power Modes

Each power mode affects the physical interface as defined in the following Table:

Table 32   Power Conditions

Mode	BSY	RDY	Interface active	Media
Active	x	x	Yes	Active
Idle	0	1	Yes	Active
Standby	0	1	Yes	Inactive
sleep	x	x	No	Inactive

Ready (RDY) is not a power condition. A device may post ready at the interface even though the media may not be accessible.

9.5 SMART Feature Set

The intent of Self-monitoring, analysis and reporting technology (SMART) is to protect user data and prevent unscheduled system downtime that may be caused by predictable degradation and/or fault of the device. By monitoring and storing critical performance and calibration parameters, SMART devices employ sophisticated data analysis algorithms to predict the likelihood of near-term degradation or fault condition. By alerting the host system of a negative reliability status condition, the host system can warn the user of the impending risk of a data loss and advise the user of appropriate action.

9.5.1 Attributes

Attributes are the specific performance or calibration parameters that are used in analyzing the status of the device. Attributes are selected by the device manufacturer based on that attribute's ability to contribute to the prediction of degrading or faulty conditions for that particular device. The specific set of attributes being used and the identity of these attributes is vendor specific and proprietary.

9.5.2 Attribute Values

Attribute values are used to represent the relative reliability of individual performance or calibration attributes. The valid range of attribute values is from 1 to 253 decimal. Higher attribute values indicate that the analysis algorithms being used by the device are predicting a lower probability of a degrading or faulty condition existing. Accordingly, lower attribute values indicate that the analysis algorithms being used by the device are predicting a higher probability of a degrading or faulty condition existing.

9.5.3 Attribute Thresholds

Each attribute value has a corresponding attribute threshold limit which is used for direct comparison to the attribute value to indicate the existence of a degrading or faulty condition. The numerical values of the attribute thresholds are determined by the device manufacturer through design and reliability testing and analysis. Each attribute threshold represents the lowest limit to which its corresponding attribute value can be equal while still retaining a positive reliability status. Attribute thresholds are set at the device manufacturer's factory and cannot be changed in the field. The valid range for attribute thresholds is from 1 through 253 decimal.

9.5.4 Threshold Exceeded Condition

If one or more attribute values, whose Pre-failure bit of their status flag is set, are less than or equal to their corresponding attribute thresholds, then the device reliability status is negative, indicating an impending degrading or faulty condition.

9.5.5 SMART Feature Set Commands

The SMART Feature Set commands provide access to attribute values, attribute thresholds and other logging and reporting information.

9.5.6 Off-Line Read Scanning

The device provides the off-line read scanning feature with reallocation. This is the extension of the off-line data collection capability. The device performs the entire read scan with reallocation for the marginal sectors to prevent the user data lost.

If interrupted by the host during the read scanning, the device services the host command.

9.5.7   Error Log

Logging of reported errors is supported. The device provides information on the last five errors that the device reported as described in SMART error log sector. The device may also provide additional vendor specific information on these reported errors. The error log is not disabled when SMART is disabled. Disabling SMART shall disable the delivering of error log information via the SMART READ LOG SECTOR command.

If a device receives a firmware modification, all error log data is discarded and the device error count for the life of the device is reset to zero.

9.5.8   Self-Test

The device provides the self-test features which are initiated by SMART Execute Off-line Immediate command. The self-test checks the fault of the device, reports the test status in Device Attributes Data and stores the test result in the SMART self-test log sector as described in SMART self-test log data structure. All SMART attributes are updated accordingly during the execution of self-test.

If interrupted by the host during the self-tests, the device services the host command.

If the device receives a firmware modification, all self-test log data is discarded.

9.6 Security Feature Set (F1h-F6h)

Security Feature Set is a powerful security feature. With a device lock password, a user can prevent unauthorized access to hard disk device even if the device is removed from the computer.

The following commands are supported for this feature.

Security Set Password ('F1'h)

Security Unlock ('F2'h)

Security Erase ('F3'h)
Prepare

Security Erase Unit ('F4'h)

Security Freeze Lock ('F5'h)

Security Disable ('F6'h)
Password

Execution of these commands is restricted for the Trusted Computing Group feature set. That is, these commands operate only in the state that is the Manufactured-Inactivate state by the Trusted Computing Group feature set. Moreover, these commands are aborted in the state that is activated to the Manufactured state by the Trusted Computing Group feature set.

9.6.1 Security Mode

Following security modes are provided.

Device Locked mode The device disables media access commands after power on. Media access commands are enabled by either a security unlock command or a security erases unit command.

Device Unlocked mode The device enables all commands. If a password is not set this mode is entered after power on, otherwise it is entered by a security unlock or a security erases unit command.

Device Frozen mode The device enables all commands except those which can update the device lock function, set/change password. The device enters this mode via a Security Freeze Lock command. It cannot exit this mode until power off.

9.6.2 Security Level

Following security levels are provided.

High level security When the device lock function is enabled and the User Password is forgotten the device can be unlocked via a Master Password.

Maximum level security When the device lock function is enabled and the User Password is forgotten then only the Master Password with a Security Erase Unit command can unlock the device. Then user data is erased.

9.6.3 Password

This function can have 2 types of passwords as described below.

Master Password When the Master Password is set, the device does NOT enable the Device Lock Function, and the device can NOT be locked with the Master Password, but the Master Password can be used for unlocking the device locked.

Identify Device Information word 92 contains the value of the Master Password Revision Code set when the Master Password was last changed. Valid values are 0001h through FFFEh.

User Password The User Password should be given or changed by a system user. When the User Password is set, the device enables the Device Lock Function, and then the device is locked on next power on reset or hard reset.

The system manufacturer/dealer who intends to enable the device lock function for the end users, must set the master password even if only single level password protection is required.

9.6.4   Operation Example

9.6.4.1   Master Password Setting

The system manufacturer/dealer can set a new Master Password from default Master Password using the 2 Set Password command, without enabling the Device Lock Function.

The Master Password Revision Code is set to FFFEh as shipping default by the HDD manufacturer

9.6.4.2   User Password Setting

When a User Password is set, the device will automatically enter lock mode the next time the device is powered on.

Figure 8   User Password - Initial Setting
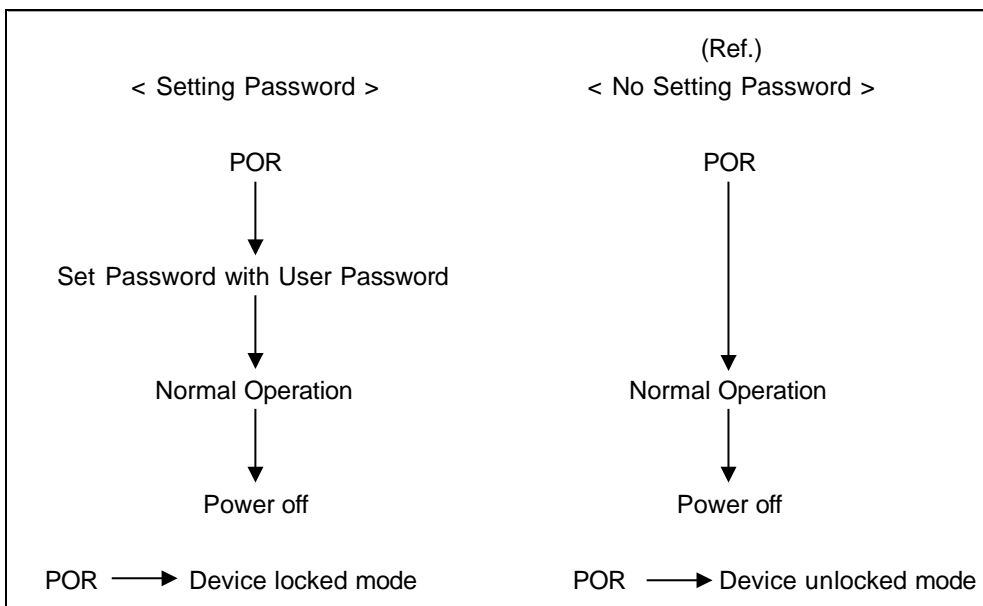
9.6.4.3   Operation from POR after User Password is Set

When Device Lock Function is enabled, the device rejects media access command until a Security Unlock command is successfully completed.

Figure 9   Usual Operation
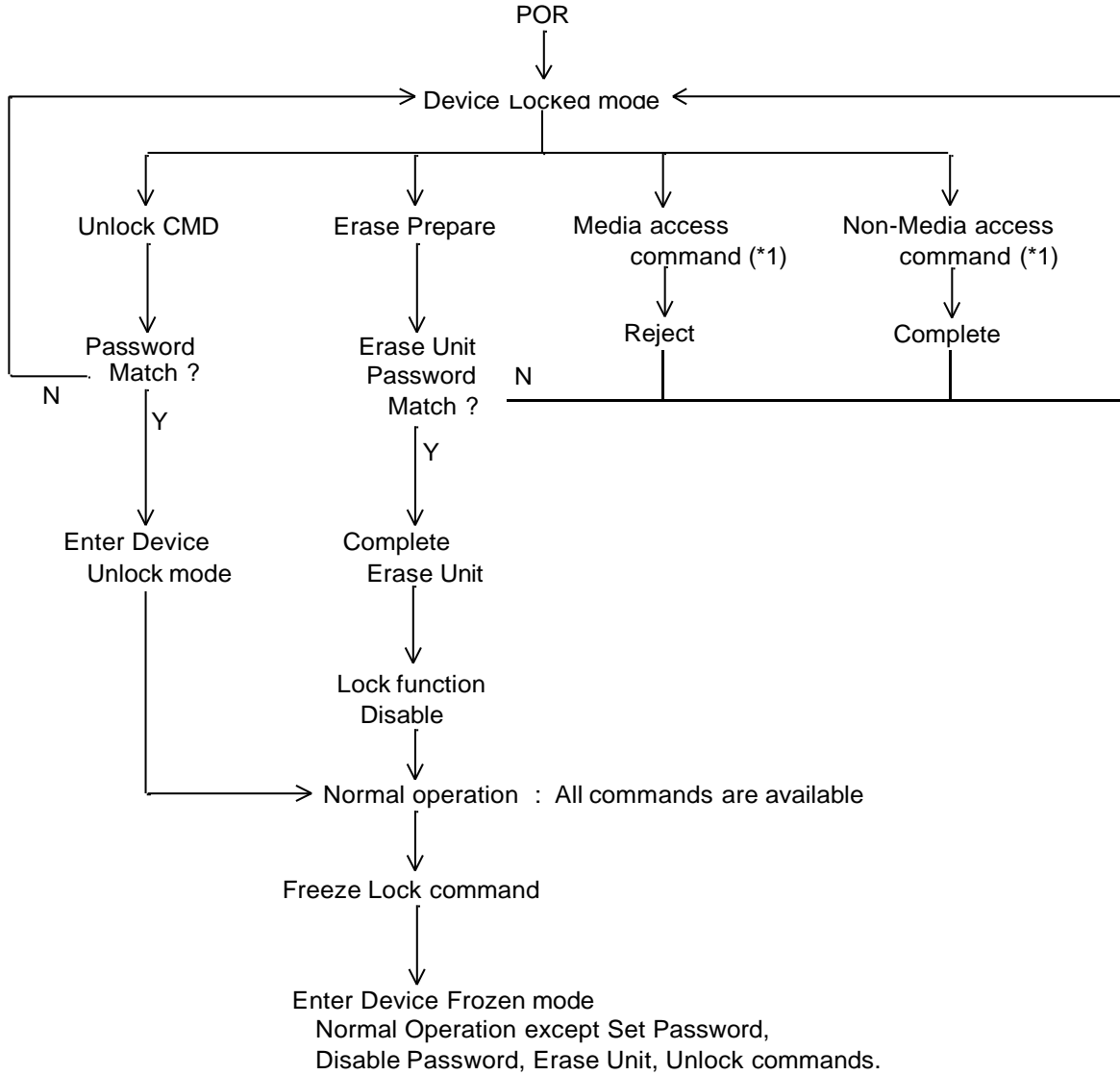
(*1) Refer to *Section 9.6.5 "Command Table"*

9.6.4.4   User Password Lost

If the User Password is forgotten and High level security is set, the system user can't access any data. However, the device can be unlocked using the Master Password.

If a system user forgets the User Password and Maximum security level is set, data access is impossible. However, the device can be unlocked using the Security Erase Unit command to unlock the device and erase all user data with the Master Password.

Figure 10   Password Lost

User Password Loat

LEVEL ? —— High ——► Unlock CMD with Master Password

Maximum

Erase Prepare Command
Erase Unit Command
with Master Password

Normal operation but data lost

Normal operation
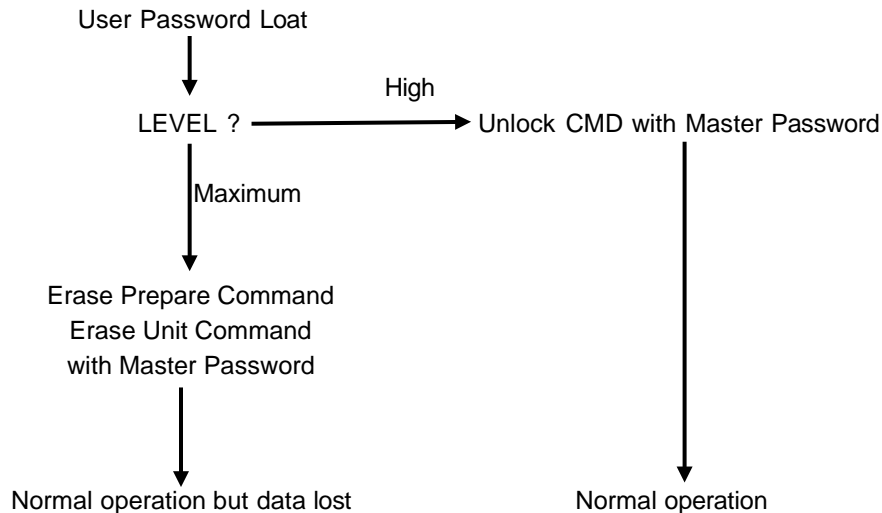
9.6.4.5   Attempt Limit for SECURITY UNLOCK Command

The SECURITY UNLOCK command has an attempt limit. The purpose of this attempt limit is to prevent that someone attempts to unlock the drive by using various passwords many times.

The device counts the password mismatch. If the password does not match, the device counts it up without distinguishing the Master password and the User password. If the count reaches 5, EXPIRE bit (bit 4) of Word 128 in Identify Device information is set, and then SECURITY ERASE UNIT command and SECURITY UNLOCK command are aborted until a hard reset or a power off. The count and EXPIRE bit are cleared after a power on reset or a hard reset.

9.6.5 Command Table

This table shows the device's response to commands when the Security Mode Feature Set (Device lock function) is enabled.

Table 33   Command Table for Device Lock Operation

Command	Locked Mode	Unlocked Mode	Frozen Mode
Check Power Mode	Executable	Executable	Executable
Download Microcode	Command aborted	Executable	Executable
Download Microcode DMA	Command aborted	Executable	Executable
Execute Device Diagnostic	Executable	Executable	Executable
Flush Cache	Command aborted	Executable	Executable
Flush Cache Ext	Command aborted	Executable	Executable
Identify Device	Executable	Executable	Executable
Idle	Executable	Executable	Executable
Idle Immediate	Executable	Executable	Executable
Initialize Device Parameters	Executable	Executable	Executable
NCQ NON-DATA	Executable	Executable	Executable
Overwrite Ext	Command aborted	Executable	Executable
Read Buffer	Executable	Executable	Executable
Read DMA	Command aborted	Executable	Executable
Read DMA Ext	Command aborted	Executable	Executable
Read FPDMA Queued	Command aborted	Executable	Executable
Read Log Ext	Executable	Executable	Executable
Read Log DMA Ext	Executable	Executable	Executable
Read Multiple	Command aborted	Executable	Executable
Read Multiple Ext	Command aborted	Executable	Executable
Read Sector(s)	Command aborted	Executable	Executable
Read Sector(s) Ext	Command aborted	Executable	Executable
Read Verify Sector(s)	Command aborted	Executable	Executable
Read Verify Sector(s) Ext	Command aborted	Executable	Executable
Recalibrate	Executable	Executable	Executable
Request Sense Data Ext	Executable	Executable	Executable
Sanitize Freeze Lock Ext	Command aborted	Executable	Executable
Sanitize Status Ext	Executable	Executable	Executable
SCT Read/Write Long	Command aborted	Command aborted	Command aborted
SCT Write Same	Command aborted	Executable	Executable
SCT Error Recovery Control	Command aborted	Executable	Executable
SCT Feature Control	Command aborted	Executable	Executable
SCT Data Table	Command aborted	Executable	Executable
SCT Read Status	Executable	Executable	Executable
Security Disable Password	Command aborted	Executable	Command aborted
Security Erase Prepare	Executable	Executable	Command aborted
Security Erase Unit	Executable	Executable	Command aborted
Security Freeze Lock	Command aborted	Executable	Executable

Security Set Password	Command aborted	Executable	Command aborted
Security Unlock	Executable	Executable	Command aborted
Seek	Executable	Executable	Executable
Set Features	Executable	Executable	Executable
Set Multiple Mode	Executable	Executable	Executable
Sleep	Executable	Executable	Executable
SMART Disable Operations	Executable	Executable	Executable
SMART Enable/Disable Attribute Autosave	Executable	Executable	Executable
SMART Enable Operations	Executable	Executable	Executable
SMART Execute Off-line Immediate	Executable	Executable	Executable
SMART Read Attribute Values	Executable	Executable	Executable
SMART Read Attribute Thresholds	Executable	Executable	Executable
SMART Return Status	Executable	Executable	Executable
SMART Save Attribute Values	Executable	Executable	Executable
SMART Read Log Sector	Executable	Executable	Executable
SMART Write Log Sector	Executable	Executable	Executable
SMART Enable/Disable Automatic Off-Line	Executable	Executable	Executable
Standby	Executable	Executable	Executable
Standby Immediate	Executable	Executable	Executable
Write Buffer	Executable	Executable	Executable
Write DMA	Command aborted	Executable	Executable
Write DMA Ext	Command aborted	Executable	Executable
Write DMA FUA Ext	Command aborted	Executable	Executable
Write FPDMA Queued	Command aborted	Executable	Executable
Write Log Ext	Command aborted	Executable	Executable
Write Log DMA Ext	Command aborted	Executable	Executable
Write Multiple	Command aborted	Executable	Executable
Write Multiple Ext	Command aborted	Executable	Executable
Write Multiple FUA Ext	Command aborted	Executable	Executable
Write Sector(s)	Command aborted	Executable	Executable
Write Sector(s) Ext	Command aborted	Executable	Executable
Write Uncorrectable Ext	Command aborted	Executable	Executable

9.7   Write Cache Function

Write Cache is a performance enhancement whereby the device reports completion of the write command (Write Sector(s), Write Multiple and Write DMA) to the host as soon as the device has received all of the data into its buffer. And the device assumes responsibility to write the data subsequently onto the disk.

- While writing data after completed acknowledgment of a write command, soft reset or hard reset does not affect its operation. But power off terminates writing operation immediately and unwritten data is lost.
- Soft reset, Standby (Immediate) command and Flush Cache commands are executed after the completion of cache flush to media. The host system can confirm the completion of write cache operation by issuing Soft reset, Standby (Immediate) command or Flush Cache command to the device before power off.

9.8   Reassign Function

The reassign Function is used with read commands and write commands. The sectors of data for reassignment are prepared as the spare data sector.

This reassignment information is registered internally, and the information is available right after completing the reassign function. Also the information is used on the next power on reset or hard reset.

If the number of the spare sector reaches 0 sectors, the reassign function will be disabled automatically.

The spare tracks for reassignment are located at regular intervals from Cylinder 0. As a result of reassignment, the physical location of logically sequenced sectors will be dispersed.

9.9   Auto Reassign Function

The sectors those show some errors may be reallocated automatically when specific conditions are met. The spare tracks for reallocation are located at regular intervals from Cylinder 0. The conditions for auto-reallocation are described below.

9.9.1   None recovered write errors
When a write operation cannot be completed after the Error Recovery Procedure (ERP) is fully carried out, the sector(s) are reallocated to the spare location. An error is reported to the host system only when the write cache is disabled and the auto reallocation is failed.

If the write cache function is ENABLED, and when the number of available spare sectors reaches 0 sectors, both auto reassign function and write cache function are disabled automatically.

9.9.2   None recovered read errors
When a read operation is failed after defined ERP is fully carried out, a hard error is reported to the host system. This location is registered internally as a candidate for the reallocation. When a registered location is specified as a target of a write operation, a sequence of media verification is performed automatically. When the result of this verification meets the criteria, this sector is reallocated.

9.9.3   Recovered read errors
When a read operation for a sector failed once then recovered at the specific ERP step, this sector of data is reallocated automatically. A media verification sequence may be run prior to the relocation according to the pre-defined conditions.

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9.10   Power-Up in Standby Feature Set

Power-Up In Standby feature set allows devices to be powered-up into the Standby power management state to minimize inrush current at power-up and to allow the host to sequence the spin-up of devices.

This feature set will be enabled/disabled via the SET FEATURES command. The enabling of this feature set shall be persistent after power cycle.

A device needs a SET FEATURES subcommand to spin-up to active state when the device has powered-up into Standby. The device remains in Standby until the SET FEATURES subcommand is received.

If power-up into Standby is enabled, when an IDENTIFY DEVICE is received while the device is in Standby as a result of powering up into Standby, the device shall set word 0 bit 2 to one to indicate that the response is incomplete, then only words 0 and 2 are correctly reported.

The IDENTIFY DEVICE information indicates the states as follows:

* identify device information is complete or incomplete
* this feature set is implemented
* this feature set is enabled or disabled
* the device needs the Set Features command to spin-up into active state

9.11   Advanced Power Management Feature Set (APM)

This feature allows the host to select an advanced power management level. The advanced power management level is a scale from the lowest power consumption setting of 01h to the maximum performance level of FEh. Device performance may increase with increasing advanced power management levels. Device power consumption may increase with increasing advanced power management levels. The advanced power management levels contain discrete bands, described in the section of Set Feature command in detail. This feature set uses the following functions:

1. A SET FEATURES subcommand to enable Advanced Power Management
2. A SET FEATURES subcommand to disable Advanced Power Management

Advanced Power Management is independent of the Standby timer setting. If both Advanced Power Management and the Standby timer are set, the device will go to the Standby state when the timer times out or the device's Advanced Power Management algorithm indicates that the Standby state should be entered.

The IDENTIFY DEVICE response word 83, bit 3 indicates that Advanced Power Management feature is supported if set. Word 86, bit 3 indicates that Advanced Power Management is enabled if set. Word 91, bits 7-0 contain the current Advanced Power Management level if Advanced Power Management is enabled.

9.12   48-bit Address Feature Set

The 48-bit Address feature set allows devices:

a) with capacities up to 281,474,976,710,655 logical sectors (i.e., up to 144,115,188,075,855,360 bytes for a 512-byte logical block device); and

b) to transfer up to 65 536 logical sectors in a single command.

The 48-bit Address feature set operates in LBA addressing only. Devices also implement commands using 28-bit addressing, and 28-bit and 48-bit commands may be intermixed.
Support of the 48-bit Address feature set is indicated in the Identify Device response bit 10 words 83. In addition, the maximum user LBA address accessible by 48-bit addressable commands is contained in Identify Device response words 230 through 233.

9.13   SATA BIST (built-in self-test)

The device supports the following BIST modes, and begins operations when it receives BIST Activate FIS.

L – Far End Retimed Loopback

T – Far End Transmit only

A – ALIGN Bypass (valid only in combination with T bit)

P – Primitive (valid only in combination with T bit)

S – Bypass Scrambling (valid only in combination with T bit)

9.14   SATA Interface Power Management

The device supports both receiving host-initiated interface power management requests and initiating interface power management. The device initiates interface power management when the device enters its power saving mode whose power consumption is lower than Idle mode.

9.14.1   Low PHY Power Conditions Overview

Low PHY power conditions are PHY conditions where the PHY is in a reduced power state (e.g., has disabled circuitry in order to reduce power). This document defines the amount of power consumed in that low PHY power condition. The low PHY power conditions include the partial PHY power condition and the slumber PHY power condition (see section **Error! Reference source not found.**).

If the partial PHY power condition is enabled and the received IDENTIFY data indicates PARTIAL mode capability, then the PHY may generate PMREQ_P (PARTIAL) primitive sequences.

If the slumber PHY power condition is enabled and the received IDENTIFY data indicates SLUMBER mode capability, then the PHY may generate PMREQ_S (SLUMBER) primitive sequences.

If low PHY power conditions are enabled, then the PHY may reply with a PMACK primitive sequence to accept a low PHY power condition request.

If low PHY power conditions are supported and disabled, then the PHY shall reject a low PHY power condition request by replying with a PMNAK primitive sequence.

9.14.2   Active PHY Power Condition

While in the active PHY power condition:

a) The PHY is capable of transmitting information and responding to received information; and

b) The PHY may consume more power than while the PHY is in a low PHY power condition.

9.14.3   Partial PHY Power Condition

The interface shall detect the OOB signaling sequence COMWAKE and COMRESET if in the Partial Interface power management state.

While in the Partial state, the interface shall be subjected to the low-transition density bit pattern (LTDP) sequences; the interface shall remain in the Partial state until receipt of a valid COMWAKE (or COMRESET) OOB signaling sequence.

Power dissipation in this Partial state shall be measured or calculated to be less than the PHY Active state, but more than the Slumber state.

The requirement for a "not-to-exceed" power dissipation limit in the Partial interface power management state is classified as vendor specific.

9.15   Slumber PHY Power Condition

The interface shall detect the OOB signaling sequence COMWAKE and COMRESET if in the Slumber Interface power management state.

While in the Slumber state, the interface shall be subjected to the low-transition density bit pattern (LTDP) sequences; the interface shall remain in the Slumber state until receipt of a valid COMWAKE (or COMRESET) OOB signaling sequence.

Power dissipation in this Slumber state shall be measured or calculated to be less than the PHY Ready state, and less than the Partial state.

The requirement for a "not-to-exceed" power dissipation limit in the Slumber interface power management state is classified as vendor specific.

9.16   Software Setting Preservation

When a device is enumerated, software will configure the device using SET FEATURES and other commands. These software settings are often preserved across software reset but not necessarily across hardware reset.   In Parallel ATA, only commanded hardware resets can occur, thus legacy software only reprograms settings that are cleared for the particular type of reset it has issued.   In Serial ATA, COMRESET is equivalent to hard reset and a non-commanded COMRESET may occur if there is an asynchronous loss of signal.   Since COMRESET is equivalent to hardware reset, in the case of an asynchronous loss of signal some software settings may be lost without legacy software knowledge.   In order to avoid losing important software settings without legacy driver knowledge, the software settings preservation ensures that the value of important software settings is maintained across a COMRESET.   Software settings preservation may be enabled or disabled using SET FEATURES with a subcommand code of 06h.   If a device supports software settings preservation, the feature shall be enabled by default.

9.16.1   COMRESET Preservation Requirements

The software settings that shall be preserved across COMRESET are listed below.   The device is only required to preserve the indicated software setting if it supports the particular feature/command the setting is associated with.

INITIALIZE DEVICE PARAMETERS: Device settings established with the INITIALIZE DEVICE PARAMETERS command.

Power Management Feature Set Standby Timer: The Standby timer used in the Power Management feature set.

Security mode state: The security mode state established by Security Mode feature set commands (refer to section 6.13 of the ATA/6 specification).   The device shall not transition to a different security mode state based on a COMRESET.   For example, the device shall not transition from the SEC5: Unlocked / not Frozen state to state SEC4: Security enabled / Locked when a COMRESET occurs, instead the device shall remain in the SEC5: Unlocked / not Frozen state.

SECURITY FREEZE LOCK: The Frozen mode setting established by the SECURITY FREEZE LOCK command. **SECURITY UNLOCK:** The unlock counter that is decremented as part of a failed SECURITY UNLOCK command attempt.

SET FEATURES (Device Initiated Interface Power Management): The Device Initiated Interface Power Management enable/disable setting (Word 79, bit 3 of Identify Device) established by the SET FEATURES command with a Subcommand code of 10h or 90h.

SET FEATURES (Write Cache Enable/Disable): The write cache enable/disable setting established by the SET FEATURES command with subcommand code of 02h or 82h.

SET FEATURES (Set Transfer Mode): PIO, Multiword, and UDMA transfer mode settings established by the SET FEATURES command with subcommand code of 03h.

SET FEATURES (Advanced Power Management Enable/Disable): The advanced power management

enable/disable setting established by the SET FEATURES command with subcommand code of 05h or 85h. The advanced power management level established in the Sector Count register when advanced power management is enabled (SET FEATURES subcommand code 05h) shall also be preserved.

SET FEATURES (Read Look-Ahead): The read look-ahead enable/disable setting established by the SET FEATURES command with subcommand code of 55h or AAh.

SET FEATURES (Reverting to Defaults): The reverting to power-on defaults enable/disable setting established by the SET FEATURES command with a subcommand code of CCh or 66h.

SET MULTIPLE MODE: The block size established with the SET MULTIPLE MODE command.

SANITIZE FREEZE LOCK MODE: The Sanitize Frozen state established by the SANITIZE FREEZE LOCK EXT command.

9.17 Serial ATA Optional Features

There following Features are Supported

9.17.1 Asynchronous Signal Recovery

The device supports asynchronous signal recovery.

9.17.2 Device Power Connector Pin 11 Definition

The device supports Pin 11 of the power connector which may be used to provide the host with an activity indication and disabling of staggered spin-up.

9.18   Phy Event Counters

Phy Event Counters are an optional feature to obtain more information about Phy level events that occur on the interface. This information may aid designers and integrators in testing and evaluating the quality of the interface. A device indicates whether it supports the Phy event counters feature in IDENTIFY (PACKET) DEVICE Word 76, bit 10. The host determines the current values of Phy event counters by issuing the READ LOG EXT command with a log page of 11h. The counter values shall not be retained across power cycles. The counter values shall be preserved across COMRESET and software resets.

The counters defined can be grouped into three basic categories: those that count events that occur during Data FIS transfers, those that count events that occur during non-Data FIS transfers, and events that are unrelated to FIS transfers. Counters related to events that occur during FIS transfers may count events related to host-to-device FIS transfers, device-to-host FIS transfers, or bi-directional FIS transfers. A counter that records bi-directional events is not required to be the sum of the counters that record the same events that occur on device-to-host FIS transfers and host-to-device FIS transfers.

Implementations that support Phy event counters shall implement all mandatory counters, and may support any of the optional counters as shown in Table 36. Note that some counters may increment differently based on the speed at which non-Data FIS retries are performed by the host and device. Implementations may record CRC and non-CRC error events differently. For example, there is a strong likelihood that a disparity error may cause a CRC error. Thus, the disparity error may cause both the event counter that records non-CRC events and the event counter that records CRC events to be incremented for the same event. Another example implementation difference is how a missing EOF event is recorded; a missing EOF primitive may imply a bad CRC even though the CRC on the FIS may be correct. These examples illustrate that some Phy event counters are sensitive to the implementation of the counters themselves, and thus these implementation sensitive counters cannot be used as an absolute measure of interface quality between different implementations.

9.18.1   Counter Reset Mechanisms

There are two mechanisms by which the host can explicitly cause the Phy counters to be reset.
The first mechanism is to issue a BIST Activate FIS to the device. Upon reception of a BIST Activate FIS the device shall reset all Phy event counters to their reset value. The second mechanism uses the READ LOG EXT command. When the device receives a READ LOG EXT command for log page 11h and bit 0 in the Features register is set to one, the device shall return the current counter values for the command and then reset all Phy event counter values.

9.18.2   Counter Identifiers

Each counter begins with a 16-bit identifier   The following Table defines the counter value for each identifier. Any unused counter slots in the log page should have a counter identifier value of 0h.
Optional counters that are not implemented shall not be returned in log page 11h. A value of '0' returned for a counter means that there have been no instances of that particular event. There is no required ordering for event counters within the log page; the order is arbitrary and selected by the device vendor.

For all counter descriptions, 'transmitted' refers to items sent by the device to the host and 'received' refers to items received by the device from the host.

Bits 14:12 of the counter identifier convey the number of significant bits that counter uses. All counter values consume a multiple of 16-bits. The valid values for bits 14:12 and the corresponding counter sizes are:

> 1h 16-bit counter
>
> 2h 32-bit counter
>
> 3h 48-bit counter
>
> 4h 64-bit counter

Any counter that has an identifier with bit 15 set to one is vendor specific. This creates a vendor specific range of counter identifiers from 8000h to FFFFh. Vendor specific counters shall observe the number of significant bits 14:12 as defined above.

Table 34   Phy Event Counter Identifiers

Identifier (Bits 11:0)	Mandatory / Optional	Description
000h	Mandatory	No counter value; marks end of counters in the page
001h	Mandatory	Command failed and ICRC bit set to one in Error register
002h	Optional	R_ERR response for Data FIS
003h	Optional	R_ERR response for Device-to-Host Data FIS
004h	Optional	R_ERR response for Host-to-Device Data FIS
005h	Optional	R_ERR response for Non-data FIS
006h	Optional	R_ERR response for Device-to-Host Non-data FIS
007h	Optional	R_ERR response for Host-to-Device Non-data FIS
008h	Optional	Not supported (Device-to-Host non-Data FIS retries)
009h	Optional	Transitions from drive PhyRdy to drive PhyNRdy
00Ah	Mandatory	Signature Device-to-Host Register FISes sent due to a COMRESET
00Bh	Optional	CRC errors within a Host-to-Device FIS
00Dh	Optional	Non-CRC errors within a Host-to-Device FIS
00Fh	Optional	Not supported (R_ERR response for Host-to-Device Data FIS due to CRC errors)
012h	Optional	Supported (R_ERR response for Host-to-Device Non-data FIS due to CRC errors)

9.18.21 Counter Definitions

The counter definitions in this section specify the events that a particular counter identifier represents.

9.18.21.1 Identifier 000h

There is no counter associated with identifier 000h. A counter identifier of 000h indicates that there are no additional counters in the log page.

9.18.21.2 Identifier 001h

The counter with identifier 001h returns the number of commands that returned an ending status with the ERR bit set to one in the Status register and the ICRC bit set to one in the Error register.

9.18.21.3 Identifier 002h

The counter with identifier 002h returns the sum of (the number of transmitted Device-to-Host Data FISes to which the host responded with R_ERRP) and (the number of received Host-to-Device Data FISes to which the device responded with R_ERRP).

9.18.21.4 Identifier 003h

The counter with identifier 003h returns the number of transmitted Device-to-Host Data FISes to which the host responded with R_ERRP.

9.18.21.5 Identifier 004h

The counter with identifier 004h returns the number of received Host-to-Device Data FISes to which the device responded with R_ERRP. The count returned for identifier 004h is not required to be equal to the sum of the counters with identifiers 00Fh and 010h.

9.18.21.6 Identifier 005h

The counter with identifier 005h returns the sum of (the number of transmitted Device-to-Host non-Data FISes to which the host responded with R_ERRP) and (the number of received Host-to-Device non-Data FISes to which the device responded with R_ERRP). Retries of non-Data FISes are included in this count.

9.18.21.7 Identifier 006h

The counter with identifier 006h returns the number of transmitted Device-to-Host non-Data FISes to which the host responded with R_ERRP. Retries of non-Data FISes are included in this count.

9.18.21.8 Identifier 007h

The counter with identifier 007h returns the number of received Host-to-Device non-Data FISes to which the device responded with R_ERRP. Retries of non-Data FISes are included in this count.

9.18.21.9 Identifier 009h

The counter with identifier 009h returns the number of times the device transitioned into the PHYRDY state from the PHYNRDY state, including but not limited to asynchronous signal events, power management events, and COMRESET events. If interface power management is enabled, then this counter may be incremented due to interface power management transitions.

9.18.21.10   Identifier 00Ah

The counter with identifier 00Ah returns the number of transmitted Device-to-Host Register FISes with the device reset signature in response to a COMRESET, which were successfully followed by an R_OK from the host.

9.18.21.11   Identifier 00Bh

The counter with identifier 00Bh returns the number of received Host-to-Device FISes of all types (Data and non-Data) to which the device responded with R_ERR$_P$ due to CRC error.

9.18.21.12   Identifier 00Dh

The counter with identifier 00Dh returns the number of received Host-to-Device FISes of all types (Data and non-Data) to which the devices responded with R_ERR$_P$ for reasons other than CRC error.

9.18.21.13   Identifier 012h

The counter with identifier 012h returns the number of received Host-to-Device FISes non- Data FISes that the device responded with R-ERRp due to CRC error. .

9.18.3 READ LOG EXT Log Page (11h)

READ LOG EXT log page 11h is one page (512 bytes) in length. The first Dword of the log page contains information that applies to the rest of the log page. Software should continue to process counters until a counter identifier with value 0h is found or the entire page has been read. A counter identifier with value 0h indicates that the log page contains no more counter values past that point. Log page 11h is defined in the Table below.

Table 35   READ LOG EXT Log Page 11h data structure definition

Byte	7	6	5	4	3	2	1	0
0	Reserved							
1	Reserved							
2	Reserved							
3	Reserved							
…	…							
n	Counter n Identifier							
n+1								
n+2	Counter n Value							
n + Counter n Length								
…	…							
508	Reserved							
509								
510								
511	Data Structure Checksum							

Counter n Identifier
  Phy event counter identifier that corresponds to Counter n Value. Specifies the particular event counter that is being reported. The Identifier is 16 bits in length.
  Valid identifiers are listed in Table 37.

Counter n Value
  Value of the Phy event counter that corresponds to Counter n Identifier. The number of significant bits is determined by Counter n Identifier bits 14:12 (as defined in Table 36). The length of Counter n Value shall always be a multiple of 16-bits. All counters are one-extended. For example, if a counter is only physically implemented as 8-bits when it reaches the maximum value of 0xFF, it shall be one-extended to 0xFFFF. The counter shall stop (and not wrap to zero) after reaching its maximum value.

Counter n Length
  Size of the Phy event counter as defined by bits 14:12 of Counter n Identifier.
  The size of the Phy event counter shall be a multiple of 16-bits.

Data Structure Checksum
  The data structure checksum is the 2's complement of the sum of the first 511 bytes in the data structure. Each byte shall be added with unsigned arithmetic and overflow shall be ignored. The sum of all 512 bytes of the data structure will be zero when the checksum is correct.

  Reserved All reserved fields shall be cleared to zero

9.18.4 NCQ NON-DATA (63h)

The NCQ NON-DATA feature allows the host to manage the outstanding NCQ commands and/or affect the processing of NCQ commands.

The NCQ NON-DATA command is a non-data NCQ command. Only specified NCQ NON-DATA subcommands are executed as Immediate NCQ commands.

NCQ NON-DATA cmd, LBA fields should not be set to reserved.

LBA fields are optionally used in SetFeatures cmd.

If NCQ is disabled and an NCQ NON-DATA command is issued to the device, then the device aborts the command with the ERR bit set to one in the Status register and the ABRT bit set to one in the Error register. This command is prohibited for devices that implement the PACKET feature set. The queuing behavior of the device depends on which subcommand is specified.

Table 36   NCQ NON-DATA - Command definition

Register	7	6	5	4	3	2	1	0
Features(7:0)	Subcommand Specific				Subcommand			
Features(15:8)	Subcommand Specific							
Count(7:0)	TAG					Reserved		
Count(15:8)	Subcommand Specific							
LBA(7:0)	Subcommand Specific							
LBA(15:8)	Subcommand Specific							
LBA(23:16)	Subcommand Specific							
LBA(31:24)	Subcommand Specific							
LBA(39:32)	Subcommand Specific							
LBA(47:40)	Subcommand Specific							
ICC(7:0)	Reserved							
Auxiliary(7:0)	Reserved							
Auxiliary(15:8)	Reserved							
Auxiliary(23:16)	Subcommand Specific							
Auxiliary(31:24)	Reserved							
Device(7:0)	Res	1	Res	0	Reserved			
Command(7:0)	63h							

Table 37 defines the Subcommand values. If an invalid subcommand is specified, then the device aborts the command with the ERR bit set to one in the Status register, the ABRT bit set to one in the Error register and causes all outstanding commands to be aborted.

Table 37   Subcommand Field

Subcommand	Description	Reference
0h	Abort NCQ queue	11.15.1 Abort NCQ Queue Subcommand (0h)
1h	Deadline Handling	11.15.2 Deadline handling Subcommand (1h)
2h - 4h	Reserved	
5h	SET FEATURES	11.15.3 Set Features Subcommand (5h)

Subcommand Specific (TTAG) is the selected queue TAG. This allows the host to select the specific outstanding queued command to be managed. The error and normal returns for this command are subcommand specific.

9.18.4.1   Abort NCQ Queue Subcommand (0h)

A Subcommand set to 0h specifies the Abort NCQ Queue subcommand (see 11.15.1 Abort NCQ Queue Subcommand (0h)). The Abort NCQ Queue subcommand is an immediate NCQ command. Support for this subcommand is indicated in the NCQ NON-DATA log (see 9.17.4.3 Read Log Ext Log Page 12h)

The Abort NCQ Queue subcommand affects only those NCQ commands for which the device has indicated command acceptance before accepting this NCQ NON-DATA command.

This command is prohibited for devices that implement the PACKET feature set.

Normal Outputs

If a supported Abort Type parameter is specified, then the device indicates success, even if the command results in no commands being aborted.

When an Abort NCQ Queue command completes successfully, a Set Device Bits FIS is sent to the host to complete the Abort subcommand and commands that were aborted as a consequence of the Abort subcommand by setting the ACT bits for those commands to one. This SDB FIS may also indicate other completed commands.

Error Outputs

The device returns command aborted if:
   a) NCQ is disabled and an Abort NCQ queue command is issued to the device;
   b) The value of the TTAG field equals the value of the TAG field;
   c) The value of the TTAG field is an invalid TAG number; or
   d) An unsupported Abort type parameter is specified.

9.18.4.2   Deadline Handling Subcommand (1h)

A Subcommand set to 1h specifies the Deadline Handling Subcommand (see 11.15.2 Deadline handling Subcommand (1h)). This subcommand controls how NCQ Streaming commands are processed by the device. Support for this subcommand is indicated in the NCQ NON-DATA Log (see 9.17.4.3 Read Read Log Ext Log Page 12h).

The state of the WDNC and RDNC bits are preserved across software resets and COMRESETs (via Software Setting Preservations), and are not preserved across power cycles.

Normal Outputs

If this Deadline Handling Subcommand command is supported, the device returns command completed with no error.

When a Deadline Handling Subcommand command completes successfully, a Set Device Bits FIS is sent to the host to complete the Deadline Handling subcommand. This SDB FIS may also indicate other completed commands.

Error Outputs

The device returns command aborted if NCQ is disabled and a Deadline Handling command is issued to the device;

SET FEATURES Subcommand (5h)

The SET FEATURES subcommand functionality and behavior is dependent on all requirements of the SET FEATURES command defined in ACS-3.

Normal Outputs

Upon successful completion of one or more outstanding commands, the device shall transmit a Set Device Bits FIS with the Interrupt bit set to one and one or more bits set to one in the ACT field corresponding to the bit position for each command TAG that has completed since the last status notification was transmitted. The ERR bit in the Status register shall be cleared to zero and the value in the Error register shall be zero.

Error Outputs

If the device has received a command that has not yet been acknowledged by clearing the BSY bit to zero and an error is encountered, the device shall transmit a Register Device to Host FIS (see Table 107) with the ERR bit set to one and the BSY bit cleared to zero in the Status field, the ATA error code in the Error field.

9.18.4.3   READ LOG EXT (12h)

To determine the supported NCQ NON-DATA subcommands and their respective features, host software reads log address 12h. This log is supported if the NCQ NON-DATA command is supported (i.e., IDENTIFY DEVICE word 77 bit 5 is set to one). Table 40 defines the 512 bytes that make up the SATA NCQ NON-DATA log. The value of the General Purpose Logging Version word is 0001h.

Table 38   NCQ NON-DATA Log (12h) data structure definition

Dword	Bits	Description
0		Subcommand 0h
	31-5	Reserved
	4	Supports Abort Selected TTAG
	3	Supports Abort Non-Streaming
	2	Supports Abort Streaming
	1	Supports Abort All
	0	Supports Abort NCQ
1		Subcommand 1h
	31-3	Reserved
	2	Supports Read Data Not Continue
	1	Supports Write Data Not Continue
	0	Supports DEADLINE HANDLING
2-4	31-0	Reserved
5		Subcommand 5h
	31-1	Reserved
	1	Supports Set Features(see 13.7.5.13)
6-127	31-0	Reserved

9.18.4.3.1   Supports the Abort NCQ Subcommand

If Supports the Abort NCQ subcommand is set to one, then the device supports the Abort NCQ Queue command (11.15.1 Abort NCQ Queue Subcommand (0h)). If Supports the Abort NCQ subcommand is cleared to zero, then the device does not support the Abort NCQ Queue command.

9.18.4.3.2   Supports Abort All

If Supports Abort All is set to one, then the device supports the value of Abort All for the Abort Type parameter of the Abort NCQ Queue command. If Supports Abort All is cleared to zero, then the device does not support the value of Abort All for the Abort Type parameter of the Abort NCQ Queue command.

9.18.4.3.3   Supports Abort Streaming

If Supports Abort Streaming is set to one, then the device supports the value of Abort Streaming for the Abort Type parameter of the Abort NCQ Queue command. If Supports Abort Streaming is cleared to zero, then the device does not support the value of Abort Streaming for the Abort Type parameter of the Abort NCQ Queue command.

9.18.4.3.4   Supports Abort Non-Streaming

If Supports Abort Non-Streaming is set to one, then the device supports the value of Abort Non-Streaming for the Abort Type parameter of the Abort NCQ Queue command. If Supports Abort Non-Streaming is cleared to zero, then the device does not support the value of Abort Non-Streaming for the Abort Type parameter of the Abort NCQ Queue command.

9.18.4.3.5   Supports the Abort Selected TTAG

If Supports Abort Selected TTAG is set to one, then the device supports the value of Abort Selected for the Abort Type parameter of the Abort NCQ Queue command. If Supports Abort Selected TTAG is cleared to zero, then the device does not support the value of Abort Selected for the Abort Type parameter of the Abort NCQ Queue command.

9.18.4.3.6   Supports the Deadline Handling Subcommand

If Supports the Deadline Handling subcommand is set to one, then the device supports the Deadline Handling command. If the Supports the Deadline Handling subcommand is cleared to zero, then the device does not support the Deadline Handling command.

9.18.4.3.7   Supports WDNC

If Supports WDNC is set to one, then the device supports the WDNC bit of the DEADLINE HANDLING command. If Supports WDNC is cleared to zero, then the device does not support the WDNC bit of the DEADLINE HANDLING command.

9.18.4.3.8   Supports RDNC

If Supports RDNC is set to one, then the device supports the RDNC bit of the Deadline Handling command. If Supports RDNC is cleared to zero, then the device does not support the WDNC bit of the Deadline Handling command.

9.18.4.3.9   Supports Set Features

If Supports Set Features is set to one, then the device supports the value of Set Features for the SET FEATURES subcommand of the NCQ NON-DATA command. If the Set Features bit is cleared to zero, then the device does not support the SET FEATURES subcommand of the NCQ NON-DATA command.

9.18.5   Rebuild Assist

The Rebuild Assist mode provides a method for a host controlling the rebuild process to determine that logical sectors on the failed device are unreadable without having to read every LBA to determine the unreadable logical sectors (i.e., the read command is terminated with an error and the failed LBA is reported in the sense data).
The storage array controller then may reconstruct the failed logical sectors.
The remaining logical sectors may be copied to the replacement device.

If the Rebuild Assist feature is enabled, then the host should issue sequential READ FPDMA QUEUED commands to extract the available data from the device.
If a READ FPDMA QUEUED command does not detect an unrecovered error, then the command should complete without error.

The Rebuild Assist feature allows reporting of an unrecovered read error or an unrecovered write error that is either predicted (i.e., a predicted unrecovered error) or unpredicted (i.e., an unpredicted unrecovered error).
If a device processes a READ FPDMA QUEUED command with the RARC bit set to one, then Rebuild Assist feature shall not affect processing of the READ FPDMA QUEUED command.

If the device processes a READ FPDMA QUEUED command with the RARC bit cleared to zero and detects a predicted unrecovered error, the following information recorded in the Queued Error log.

A)   The Sense Key field is set to Bh(ABORTED COMMAND);

B)   The Additional Sense Code field and the Additional Sense Code Qualifier field is set to 1103h (MULTIPLE READ ERRORS);

C)   The LBA field is set to the LBA of the first unrecovered logical sector; and

D)   The Final LBA In Error field is set to the LBA of the last predicted unrecovered logical sector in a sequence of contiguous unrecovered logical sectors that started with the first LBA in error.

9.18.5.1   Rebuild Assist Log (log page 15h)

If the device supports the Rebuild Assist feature (i.e., IDENTIFY DEVICE data Word 78 bit 11 is set to one), then the Rebuild Assist log shall be supported.

Table 39   Rebuild Assist log (15h) data structure definition

Byte	7	6	5	4	3	2	1	0
0	Reserved							Rebuild Assist Enabled
1…6	Reserved							
7	Physical Element Length (N)							
8	(MSB)							
	Disabled Physical Element Mask							
7 + N								(LSB)
8 + N	(MSB)							
	Disabled Physical Elements							
7+(2×N)								(LSB)
8+(2×N)..511	Reserved							

Physical Element Length
The Physical Element Length field indicates the number of bytes in the Disabled Physical Element Mask field and the number of bytes in the Disabled Physical Elements field.
The device shall ignore any attempt by the host to change the value of this field when writing to the Rebuild Assist log.

Disabled Physical Element Mask
The Disabled Physical Element Mask field indicates that bits in the Disabled Physical Elements field are supported.
The device shall ignore any attempt by the host to change the value of this field when writing to the Rebuild Assist log.

Disabled Physical Elements

The Disabled Physical Elements field specifies if physical elements shall be disabled. Each bit that is set to one in the Disabled Physical Elements field specifies that LBAs associated with this physical element shall respond to read commands and write commands as if the associated LBAs have predicted errors.

Each bit that is set to zero in the Disabled Physical Elements field specifies that LBAs associated with this physical element shall respond to read commands and write commands as if the associated LBAs do not have predicted errors.

9.18.5.2　Enabling the Rebuild Assist Feature

If the host writes to the Rebuild Assist log and sets the Rebuild Assist Enabled field to one, then:
a) The device will initiate a self-test of the physical elements contained within the device and should disable any physical elements that are not functioning correctly;
b) The device shall initialize the Disabled Physical Elements from the results of the self-test;
c) The device shall minimize device-initiated background activities; and
d) The device shall enable the Rebuild Assist feature. The host may verify that Rebuild Assist feature is enabled by reading the Rebuild Assist log, and then examining the data returned and verifying that the Rebuild Assist Enabled field is set to one

9.18.5.3　Using the Rebuild Assist Feature Overview

If the Rebuild Assist feature is enabled, then the host should issue sequential READ FPDMA QUEUED commands to extract the available data from the device. If a READ FPDMA QUEUED command does not detect an unrecovered error, then the command should complete without error.

The Rebuild Assist feature allows reporting of an unrecovered read error or an unrecovered write error that is either predicted (i.e., a predicted unrecovered error) or unpredicted (i.e., an unpredicted unrecovered error). If a device processes a READ FPDMA QUEUED command with the RARC bit set to one, then Rebuild Assist feature shall not affect processing of the READ FPDMA QUEUED command.

9.18.5.4　Disabling the Rebuild Assist Feature

If the device supports the Rebuild Assist feature (i.e., IDENTIFY DEVICE data Word 78 bit 11 is set to one), then The Rebuild Assist feature shall be disabled if:

a) The device processes a power cycle; or

b) The device processes a command to write to the Rebuild Assist log (see 13.7.8) with the Rebuild Assist Enabled bit cleared to zero.

9.18.6　Power Disable

The Power Disable feature is optional. If supported and enabled, the Power Disable feature may be used to disable power to the device circuitry which enables a system that supports this feature to perform a hard reset of the drive.

When deploying drives in systems that do not support this feature, it is recommended that you select part numbers without this option.

9.19   SCT Command Transport Feature Set

9.19.1   Overview

9.19.1.1   Introduction

SMART Command Transport (SCT) is the method for the drive to receive commands using log page E0h and transporting data using log page E1h. These log pages are used as follows:

Table 40   SCT Log Page and Direction

	Log page E0h	Log Page E1h
Write log page	Issue Command	Send Data to the drive
Read log page	Return Status	Received Data from the drive

There are two ways to access the log pages: using SMART READ/WRITE LOG and READ/WRITE LOG EXT. Both sets of commands access the same log pages and provide the same capabilities.

The log directory for log pages E0h and E1h should report a length of one. The length of log page E1h does not indicate the length of an SCT data transfer.

If SMART is supported, but not enabled, the drive supports SMART READ/WRITE LOG for Log page E0h and E1h.

If security is enabled and password has not been issued to unlock the device, all SCT commands will fail.

9.19.1.2   Capability Definition

Capability Identification is performed by issuing Identify Device command. Word 206 of Identify Data is used to determine if SCT is enabled and which SCT Action Codes are supported.

Table 41   Identify Device Information Word 206

Word	Description	
206	SCT Command set support	
	15-12	Vendor Specific
	11-6	Reserved
	5	Action Code 5 (SCT Data Table) supported
	4	Action Code 4 (Features Control) supported
	3	Action Code 3 (Error Recovery Control) supported
	2	Action Code 2 (SCT Write Same) supported
	1	Obsolete
	0	SCT Feature Set supported (includes SCT status)

9.19.1.3   SCT Command Nesting and Intermingling with Standard Commands

In general, standard ATA commands can be intermingled with SCT Commands but SCT commands cannot be nested.

SCT commands that do require a follow-on data transfer operation never have an issue with being intermixed with any ATA commands or each other.

SCT commands that do require data transfer, on the other hand, may not be nested; that is, if a key command that requires a data transfer is issued, all data transfer – to or from the host – must complete before another SCT command is issued. In most cases, however, ATA read/write commands may be inserted in between SCT data transfers, that is, between complete SMART Read Log/Write Log commands.   Furthermore, any reset (power-on, software or hardware) will cause the SCT command to be aborted.

9.19.1.4 Resets

If an SCT command is executing, any reset including Soft Reset, Hard Reset, COMRESET, and Power-On Reset all cause the command to be terminated. This could result in partial command execution or data loss. There is no indication once the drive becomes ready that the previous command was terminated.

9.19.2   SCT Command Protocol

9.19.2.1   Command Transport

SCT Command Transport occurs when a 512-byte data packet (called "Key Sector") is created and the written to SMART or extended log page E0h. The key sector specifies Action and Function Codes along with the parameters that are required to perform the action.

9.19.2.1.1   Issue SCT Command Using SMART

Table 42   Output Registers of SCT Command Using SMART

Command Block Output Registers									
Register	7	6	5	4	3	2	1	0
Feature	D6h							
Sector Count	01h							
Sector Number	E0h							
Cylinder Low	4Fh							
Cylinder High	C2h							
Device/Head	-	-	-	D	-	-	-	-
Command	B0h							

Table 43   Input Registers of SCT Command Using SMART

Command Block Input Registers (Success)										Command Block Input Registers (Error)									
Register	7	6	5	4	3	2	1	0	Register	7	6	5	4	3	2	1	0
Error	00h								Error	04h							
Sector Count	Depends on command (LSB)								Sector Count	Extended Status code (LSB)							
Sector Number	Depends on command (MSB)								Sector Number	Extended Status code (MSB)							
Cylinder Low	Number of sectors to transfer (LSB)								Cylinder Low	Number of sectors to transfer (LSB)							
Cylinder High	Number of sectors to transfer (MSB)								Cylinder High	Number of sectors to transfer (MSB)							
Device/Head	-	-	-	-	-	-	-	-	Device/Head	-	-	-	-	-	-	-	-
Status	50h								Status	51h							

9.19.2.1.2   Issue SCT Command Using Write Log Ext

Table 44   Input Registers of SCT Command Using Write Log Ext

Command Block Output Registers										
Register		7	6	5	4	3	2	1	0	
Feature	Current	Reserved								
	Previous	Reserved								
Sector Count	Current	01h								
	Previous	00h								
LBA Low	Current	E0h								
	Previous	Reserved								
LBA Mid	Current	00h								
	Previous	00h								
LBA High	Current	Reserved								
	Previous	Reserved								
Device/Head		-	-	-	D	-	-	-	-	
Command		3Fh								

Table 45   Output Registers of SCT Command Using Write Log Ext

Command Block Input Registers (Success)											Command Block Input Registers (Error)										
Register		7	6	5	4	3	2	1	0		Register		7	6	5	4	3	2	1	0	
Error		00h									Error		04h								
Sector Count	HOB=0	Depends on command (LSB)									Sector Count	HOB=0	Extended Status Code (LSB)								
	HOB=1	Reserved										HOB=1	Reserved								
LBA Low	HOB=0	Depends on command (MSB)									LBA Low	HOB=0	Extended Status Code (MSB)								
	HOB=1	Reserved										HOB=1	Reserved								
LBA Mid	HOB=0	Number of sectors (LSB)									LBA Mid	HOB=0	Number of sectors (LSB)								
	HOB=1	Reserved										HOB=1	Reserved								
LBA High	HOB=0	Number of sectors (MSB)									LBA High	HOB=0	Number of sectors (MSB)								
	HOB=1	Reserved										HOB=1	Reserved								
Device/Head		-	-	-	-	-	-	-	-		Device/Head		-	-	-	-	-	-	-	-	
Status		50h									Status		51h								

All ATA "previous" registers are reserved in Write Log Ext responses.

9.19.2.1.3　Key Sector Format

An SCT command (Key Sector) is always 512 bytes long. Table below shows the generic format of an SCT command.

Table 46　Key Sector Format

Byte	Field	Words	Description
1:0	Action Code	1	This field defines the command type and generally specifies the type of data being accessed, such as sector or physical action being performed, such as seek.
3:2	Function Code	1	This field specifies the type of access, and varies by command. For example, this can specify read, write, verify, etc.
X:4	Parameter1	Depends on command	Depends on command
Y:x+1	Parameter2	Depends on command	Depends on command
…	…	…	…
	Total Words	256	

The action codes are defined in Table below.

Table 47　SCT Action Code List

Action Code	Block Data	TF Data	Description
0000h	-	-	Reserved
0001h	Read/Write	Y	Long Sector Access　　(Not Supported)
0002h	Write	N	SCT Write Same
0003h	-	Y	Error Recovery Control
0004h	-	Y	Features Control
0005h	Read	N	SCT Data Table
0006h-BFFFh	-	-	Reserved
C000h-FFFFh	-	-	Vendor Specific

9.19.2.1.4 Extended Status Code

Table 48 Extended Status Code

Status Code	Definition
0000h	Command complete without error
0001h	Invalid Function Code
0002h	Input LBA out of range
0003h	Request sector count overflow. The number of sectors requested to transfer (Sector Count register) in the read or write log command is larger than required by SCT command.
0004h	Invalid Function code in Error Recovery command
0005h	Invalid Selection code in Error Recovery command
0006h	Host read command timer is less than minimum value
0007h	Host write command timer is less than minimum value
0008h	Background SCT command was aborted because of an interrupting host command
0009h	Background SCT command was terminated because of unrecoverable error
000Ah	Invalid Function code in Long Sector Access command
000Bh	SCT data transfer command was issued without first issuing an SCT command
000Ch	Invalid Function code in Feature Control command
000Dh	Invalid Feature code in Feature Control command
00Eh	Invalid New State value in Feature Control command
000Fh	Invalid Option Flags in Feature Control command
0010h	Invalid SCT Action code
0011h	Invalid Table ID (table not supported)
0012h	Command was aborted due to drive security being locked
0013h	Invalid revision code
0015h	The most recent non-SCT command returned command completion with an error due to the SCT Error Recovery Control Read Command Timer or SCT Error Recovery Control Write Command Timer expiring
0017h	Blocking SCT Write Same command was terminated because of unrecoverable error
0018h-BFFFh	Reserved
C000h-C002h	Vendor Specific
C003h	Overlay switch failure in Long Sector Access command
C004h	Read Long failure
C005h	Write Long failure
C006h	Write Cache enable failure
C007h-FFEFh	Vendor Specific
FFF0h-FFFEh	Reserved
FFFFh	SCT command executing in background

9.19.2.2   Data Transfer

Once an SCT command has been issued, status can be checked and data can be transferred. Data transfer uses log page E1h.

9.19.2.2.1   Read/Write SCT Data Using SMART

Table 49   Input Registers of SCT Data Transfer Using SMART

Command Block Output Registers									
Register	7	6	5	4	3	2	1	0	
Feature	D5h(Read)/D6h(Write)								
Sector Count	Number of sectors to be transferred								
Sector Number	E1h								
Cylinder Low	4Fh								
Cylinder High	C2h								
Device/Head	-	-	-	D	-	-	-	-	
Command	B0h								

9.19.2.2.2   Read/Write SCT Data Using Read/Write Log Ext

Table 50   Input Registers of SCT Data Transfer using Read/Write Log Ext

Command Block Output Registers										
Register		7	6	5	4	3	2	1	0	
Feature	Current	Reserved								
	Previous	Reserved								
Sector Count	Current	01h or 08h								
	Previous	00h								
LBA Low	Current	E1h								
	Previous	Reserved								
LBA Mid	Current	00h								
	Previous	00h								
LBA High	Current	Reserved								
	Previous	Reserved								
Device/Head		-	-	-	D	-	-	-	-	
Command	2Fh(Read)/3Fh(Write)									

9.19.2.3   SCT Status Request

Once an SCT command has been issued, a status is reported in the ATA registers. This status indicates that the command was accepted or that an error occurred. This ATA status return does not indicate successful completion of the SCT actions. Some commands can take several minutes or even hours to execute. In this case, the host can determine execution progress by requesting SCT status.

Log page E0h contains the status information. Reading log page E0h retrieves the status information. The SCT status may be acquired any time that the host is allowing to send a command to the device. This command will not change the power state of the drive, nor terminate any background activity, including any SCT command in progress.

9.19.2.3.1   SCT Status Request Using SMART

Table 51   Input Registers of SCT Status Request Using SMART

Command Block Output Registers									
Register	7	6	5	4	3	2	1	0	
Feature	D5h								
Sector Count	01h								
Sector Number	E0h								
Cylinder Low	4Fh								
Cylinder High	C2h								
Device/Head	-	-	-	D	-	-	-	-	
Command	B0h								

9.19.2.3.2   SCT Status Request Using Read Log Ext

Table 52   Input Registers of SCT Status Request Using Read Log Ext

Command Block Output Registers										
Register		7	6	5	4	3	2	1	0	
Feature	Current	Reserved								
	Previous	Reserved								
Sector Count	Current	01h								
	Previous	00h								
LBA Low	Current	E0h								
	Previous	Reserved								
LBA Mid	Current	00h								
	Previous	00h								
LBA High	Current	Reserved								
	Previous	Reserved								
Device/Head		-	-	-	D	-	-	-	-	
Command		2Fh								

9.19.2.3.3 Format of SCT Status Response

Table 53   Data Format of SCT Status Response -1

Byte	Type	Field Name	Value	Description
1:0	Word	Format Version	0003h	Status Response format version number
3:2	Word	SCT Version		Manufacturer's vendor specific implementation version number
5:4	Word	SCT Spec.	0001h	Highest level of SCT Technical Report supported
9:6	Dword	Status Flags		Bit 0 : Segment Initialized Flag If this bit is set to 1, an SCT Write Same command write to all LBAs of the drive has completed without error. This bit shall be cleared to 0 when any user LBA is written, even if write cache is enabled. This bit is else cleared if the capacity of the drive is changed via SETMAX, SETMAX EXT or DCO. This bit is preserved through a power cycle. Bit 1-31 : Reserved
10	Byte	Drive Status		0 = Active waiting for a command 1 = Stand-by 2 = Sleep 3 = DST executing in background 4 = SMART ODC executing in background 5 = SCT executing in background
13:11	Byte[3]	reserved	00h	
15:14	Word	Extended Status Code		Status Of last SCT command issued. FFFFh if SCT command executing in background.
17:16	Word	Action Code		Action code of last SCT command issued. If the Extended Status Code is FFFFh, this is the Action Code of the command that is current executing.
19:18	Word	Function Code		Function code of last SCT command issued. If the Extended Status Code is FFFFh, this is the Function Code of the command that is current executing.
39:20	Byte[20]	reserved	00h	
47:40	Qword	LBA		Current LBA of SCT command execution in background. If there is no command currently executing in the background, this field is undefined.
199:48	Byte[152]		00h	
200	Byte	HDA Temp		Current HDA temperature in degrees Celsius. This is a 2's complement number. 80h indicates that this value is invalid.
201	Byte	Min Temp		Minimum HDA temperature in degrees Celsius. This is a 2's complement integer. 80h indicates that this value is invalid.
202	Byte	Max Temp		Maximum HDA temperature in degrees Celsius. This is a 2's complement number. 80h indicates that this value is invalid.
203	Byte	Life Min Temp		Minimum HDA temperature in degrees Celsius seen for the life of the device. This is a 2's complement integer. 80h indicates that this value is invalid.
204	Byte	Life Max Temp		Maximum HDA temperature in degrees Celsius seen for the life of the drive. This is a 2's complement number. 80h indicates that this value is invalid.

Table 54   Data Format of SCT Status Response -2

Byte	Type	Field Name	Value	Description
205	Byte	Reserved	00h	
209:206	Dword	Over Limit Count		Number of temperature recording Intervals since the last power-on reset where the recorded temperature was greater than Max Op Limit. See table 93 for information about this Interval.
213:210	Dword	Under Limit Count		Number of temperature recording Intervals since the last power-on reset where the recorded temperature was less than Min Op Limit. See table 93 for information about this Interval.
479:214	Byte[275]	Reserved	00h	
511:480	Byte[32]	Vendor Specific	00h	

9.19.3 SCT Command Set

9.19.3.1 SCT Write Same (action code : 0002h)

Inputs: (Key Sector)

Table 55 SCT Write Same (Inputs

Word	Name	Value	Description
0	Action Code	0002h	This action writes a pattern or sector of data repeatedly to the media. This capability could also be referred to as "Write All" or "Write Same".
1	Function Code	0001h	Repeat Write Pattern (Background Operation)
		0002h	Repeat Write Sector (Background Operation)
		0003h	Repeat Write one or more Sectors (Background Operation)
		0101h	Repeat Write Pattern (Blocking Operation)
		0102h	Repeat Write Sector (Blocking Operation)
5:2	Start LBA	Qword	First LBA
9:6	Count	Qword	Number of sectors to fill
11-10	Pattern	Dword	If the Function Code is 0001h, this field contains a 32-bit pattern that is written on the media starting at the location specified in words two through five
15-12	Pattern Length	Qword	If function code is 00003h, this field contains the number of logical sectors in the pattern sent by the host.

Outputs: (TF Data)

Table 56 Output Registers of SCT Write Same (Success

Command Block Input Registers (Success)	
Error	00h
Sector Count	Reserved
Sector Number	Reserved
Cylinder Low	Number of sectors to transfer (LSB) = 01h
Cylinder High	Number of sectors to transfer (MSB) = 00h
Device/Head	Reserved
Status	50h

The SCT Write Same command will begin writing sectors from Start LBA in incrementing order until Count sectors have been written. A Count of zero means apply operation from Start LBA until the last user LBA on the drive is reached. The HPA feature determines the last user LBA. This command will not write over a hidden partition when hidden partitions are enabled using the Host Protected Area drive capabilities. Automatic sector reassignment is permitted during the operation of this function.

If Start LBA or Start LBA + Count go beyond the last user LBA then an error is reported and the SCT command is not executed. Issuing this command with a value of zero for Start LBA and Count will cause all LBAs of the drive to be written the specified pattern.

Once the key sector has been issued, if the Function Code was 0002h or 0102h and the TF Data indicates that the drive is ready to receive data, log page E1h should be written to transfer the data.

This command can change the Segment Initialized Flag. If the command writes all the user addressable sectors and completes without encountering an error or being aborted, then the "Segment Initialized Flag" (bit 0 of the Status Flags in the SCT Status. See Table 55) shall be set to 1. A write to any user addressable sector on the drive

(except another complete write all), shall cause the Segment Initialized Flag to be cleared. Reallocations as a result of reading data (foreground or background) do not clear the Segment Initialized Flag.

Implementation note for Background Operation (Function code = 0001h, 0002h)

In this mode, the drive will return command completion status when the drive finished receiving data.

Any command, including IDENTIFY DEVICE, other than SCT Status, issued to the drive while this command is in progress will terminate the SCT Write Same command. The incoming command is executed.

Use the SCT Status command to retrieve status information about the current SCT command. Example status information includes: command active or complete, current LBA, and errors. When this command is in progress, the SCT status error code will be FFFFh, and set to 0000h if the command completes without error. It will be less than FFFFh and grater the 0000h if the command terminated prematurely for any reason.

Possible Extended Status Code for Background Operation (Function code = 0001h, 0002h)	
0008h	Background SCT command was aborted because of an interrupting host command
0009h	Background SCT command was terminated because of unrecoverable error
FFFFh	SCT command executing in background

Implementation note for Blocking Operation (Function code = 0101h, 0102h)

In this mode, the drive will return command completion status when the drive finished the SCT Write Same operation.

Outputs for Error

Table 57   Output Registers of SCT Write Same (Error)

Command Block Input Registers (Error)								
Register	7	6	5	4	3	2	1	0
Error	04h							
Sector Count	Extended Status code (LSB)							
Sector Number	Extended Status code (MSB)							
Cylinder Low	N/A							
Cylinder High	N/A							
Device/Head	-	-	-	-	-	-	-	-
Status	51h							

Possible Extended Status Code for Blocking Operation (Function code = 0101h, 0102h)	
0017h	Blocking SCT Write Same command was terminated because of unrecoverable error

9.19.3.2　Error Recovery Control Command (action code : 0003h)

Inputs: (Key Sector)

Table 58　Error Recovery Control Command (Inputs)

Word	Name	Value	Description
0	Action Code	0003h	Set the read and write error recovery time
1	Function Code	0001h	Set New Value
		0002h	Return Current Value
2	Selection Code	0001h	Read Timer
		0002h	Write Timer
3	Value	Word	If the function code is 0001h, then this field contains the recovery time limit in 100ms units. The minimum SCT timeout value is 65 (=6.5 second). When the specified time limit is shorter than 6.5 second, the issued command is aborted.
255:4	reserved	0000h	

Outputs: (TF Data)

Table 59　Error Recovery Control Command (On puts)

Command Block Input Registers (Success)	
Error	00h
Sector Count	If Function Code was 0002h, then this is the LSB of the requested recovery limit. Otherwise, this field is reserved.
Sector Number	If Function Code was 0002h, then this is the MSB of the requested recovery limit. Otherwise, this field is reserved.
Cylinder Low	reserved
Cylinder High	reserved
Device/Head	reserved
Status	50h

The Error Recovery Control command can be used to set time limits for read and write error recovery. For non-queued commands, these timers apply to command completion at the host interface. For queued commands where in order data delivery is enabled, these timers begin counting when the device begins to execute the command, not when the command is sent to the device. These timers do not apply to streaming commands, or to queued commands when out-of-order data delivery is enabled.

These command timers are volatile. The default value is 0 (i.e. disable command time-out).

If a Read Command Timer expires or a Write Command Timer expires before command completion, the device:

a) Shall stop processing that command and return an error;

b) Shall return an Uncorrectable Error, if that command was a read command;

c) Should return command aborted, if that command was a write command; and

d) Should set the EXTENDED STATUS CODE field to 0015h (see Table 50)

The EXTENDED STATUS CODE field shall be cleared during the processing of the next non-SCT command by the device, except if the command being processed is a read of the NCQ Command Error log.

9.19.3.3 Feature Control Command (action code : 0004h)

Inputs: (Key Sector)

Table 60 Feature Control Command (Inputs)

Word	Name	Value	Description
0	Action Code	0004h	Set or return the state of drive features described in Table 64
1	Function Code	0001h	Set state for a feature
		0002h	Return the current state of a feature
		0003h	Return feature option flags
2	Feature Code	Word	See Table 64 for a list of the feature codes
3	State	Word	Feature code dependent value
4	Option Flags	Word	Bit15:1 = Reserved If the function code is 0001h, setting bit 0 to one causes the requested feature state change to be preserved across power cycles. If the function code is 0001h, setting bit 0 to zero causes the requested feature state change to be volatile. A hard reset causes the drive to revert to default, or last non-volatile setting.
255:5	reserved	0000h	

Outputs: (TF Data)

Table 61 Feature Control Command (Outputs)

Command Block Input Registers (Success)	
Error	00h
Sector Count	If Function Code was 0002h, then this is the LSB of Feature State. If Function Code was 0003h, then this is the LSB of Option Flags. Otherwise, this field is reserved.
Sector Number	If Function Code was 0002h, then this is the MSB of Feature State. If Function Code was 0003h, then this is the MSB of Option Flags. Otherwise, this field is reserved.
Cylinder Low	reserved
Cylinder High	reserved
Device/Head	reserved
Status	50h

Table 62 Feature Code List

Feature Code	State Definition
0001h	0001h : Allow write cache operation to be determined by Set Feature command
	0002h : Force write cache enabled
	0003h : Force write cache disabled
	If State 0001h is selected, the ATA Set Feature command will determine the operation state of write cache. If State 0002h or 0003h is selected, write cache will be forced into the corresponding operation state, regardless of the current ATA Set Feature state. Any attempt to change the write cache setting through Set Feature shall be accepted, but otherwise ignored, and not affect the operation state of write cache and complete normally without reporting an error.
	In all cases, bit 5 of word 85 in the Identify Device information will reflect the true operation state of write cache, one indicating enabled and zero indicating disabled.
	The default state is 0001h.
0002h	0001h : Enable Write Cache Reordering
	0002h : Disable Write Cache Reordering
	The default state is 0001h.
	The drive does not return error for setting state 0002h, but the state is ignored.
0003h	Set time interval for temperature logging.
	0000h is invalid.
	0001h to FFFFh logging interval in minutes.
	This value applies to the Absolute HDA Temperature History queue. Issuing this command will cause the queue to be reset and any prior values in the queue will be lost. Queue Index shall be set to zero and the first queue location will be set to the current value. All remaining queue locations are set to 80h. The Sample Period, Max Op Limit, Over Limit, Min Op Limit and Under Limit values are preserved.
	Default value is 0001h.
0004h-CFFFh	Reserved
D000h-FFFFh	Vendor Specific

9.19.3.4   SCT Data Table Command (action code : 0005h)

Inputs: (Key Sector)

Table 63   SCT Data Table Command (Inputs)

Word	Name	Value	Description
0	Action Code	0005h	Read a data table
1	Function Code	0001h	Read Table
2	Table ID	Word	See Table 67 for a list of data tables
255:2	reserved	0000h	

Outputs: (TF Data)

Table 64   SCT Data Table Command (Outputs)

Command Block Input Registers (Success)	
Error	00h
Sector Count	reserved
Sector Number	reserved
Cylinder Low	Number of sectors to transfer (LSB) = 01h
Cylinder High	Number of sectors to transfer (MSB) = 00h
Device/Head	reserved
Status	50h

Table 65   Table ID

Table ID	Description
0000h	Invalid
0001h	Reserved
0002h	HDA Temperature History Table (in absolute degree C). See Table 69
0003h-CFFFh	Reserved
D000h-FFFFh	Vendor Specific

Table 66   Data Format of HDA Absolute Temperature History Table-1

Byte	Size	Field Name	Description
1:0	Word	Format Version	Data table format version (=0002h)
3:2	Word	Sampling Period	Absolute HDA Temperature sampling period in minutes. 0000h indicates sampling is disabled.
5:4	Word	Interval	Timer interval between entries in the history queue.
6	Byte	Max Op Limit	Maximum recommended continuous operating temperature. This is a one byte 2's complement number that allows a range from -127°C to +127°C to be specified. 80h is an invalid value. This is a fixed value.
7	Byte	Over Limit	Maximum temperature limit. This is a one byte 2's complement number that allows a range from -127°C to +127°C to be specified. 80h is an invalid value. This is a fixed value.
8	Byte	Min Op Limit	Minimum recommended continuous operating limit. This is a one byte 2's complement number that allows a range from -127°C to +127°C to be specified. 80h is an invalid value. This is a fixed value.
9	Byte	Under Limit	Minimum temperature limit. This is a one byte 2's complement number that allows a range from -127°C to +127°C to be specified. 80h is an invalid value. This is a fixed value.
29:10	Byte[20]	Reserved	
31:30	Word	Queue Size	Number of entry locations in history queue. This value is 128.
33:32	Word	Queue Index	Last updated entry in queue. Queue Index is zero-based, so Queue Index 0000h is the first location in the buffer (at offset 34). The most recent temperature entered in the buffer is at Queue Index + 34. See Note 1 and Note 2.

Table 67   Data Format of HDA Absolute Temperature History Table-2

Byte	Size	Field Name	Description
(Queue Size+33):34	Byte[Queue Size]	Queue Buffer	This is a circular buffer of absolute HDA Temperature values. These are one byte 2's complement numbers, which allow a range from -127°C to +127°C to be specified. A value of 80h indicates an initial value or a discontinuity in temperature recording.
			The Actual time between samples may vary because commands may not be interrupted. The sampling period is the minimum time between samples. See Note 1.
			If the host changes the logging interval using the volatile option, the interval between entries in the queue may change between power cycles with no indication to the host.
511 (Queue Size +34)	Byte [512-Queue Size-34]	Reserved	

Note 1 – The Absolute HDA Temperature History is preserved across power cycles with the requirement that when the drive powers up, a new entry is made in the history queue of 80h, an invalid absolute temperature value. This way an application viewing the history can see the discontinuity in temperature result from the drive being turned off.

Note 2 – When the Absolute HDA Temperature history is cleared, for new drives or after changing the Logging Interval, the Queue Index shall be set to zero and the first queue location shall be set to the current Absolute HDA Temperature value. All remaining queue locations are set to 80h.

9.20 Extended Power Conditions (EPC) Feature

The Extended Power Conditions feature set provides a host with additional methods to control the power condition of a device.

Subcommand code 4Ah enables, disables, and configures the use of the Extended Power Conditions feature set. If the EPC feature set is not supported, then the device return command aborted Table 70 describes the EPC subcommands and Table 71 describes the Power Condition IDs.

Table 68   Extended Power Conditions Subcommands

EPC Subcommand	Description
0h	Restore Power Condition Settings
1h	Go To Power Condition
2h	Set Power Condition Timer
3h	Set Power Condition State
4h	Enable the EPC feature
5h	Disable the EPC feature
6h … Fh	Reserved

Table 69   Power Condition IDs

Power Condition ID	Power Condition Name	Description
00h	standby_z	Standby
01h	standby_y	Low RPM Idle
02h…80h		Reserved
81h	idle_a	Active Idle
82h	idle_b	Low Power Idle
83h	idle_c	Low RPM Idle
84h … FEh		Reserved
FFh	All	All supported EPC power conditions

9.20.1 Power Conditions

idle_a, idle_b and idle_c are power conditions within the PM1:Idle power management state. standby_y and standby_z are power conditions within the PM2:Standby power management state. Please refer to ACS-4 Definitions and abbreviations" about PM1:Idle and PM2:Standby. The power conditions are ordered from highest power consumption (i.e., shortest recovery time) to lowest power consumption (i.e., longest recovery time) as follows:

Idle_A power → Idle_B power → Idle_C power → Standby_Y power → Standby_Z power

Each of these power conditions has a set of current, saved and default settings. Default settings are not modifiable. Default and saved settings persist across power cycles. The current settings do not persist across power cycles.

9.20.2   Power Condition Timers

The device has manufacturer specified power-on default settings for the power condition timers. Power condition timers are changeable with the SET FEATURES Extended Power Conditions subcommand.
A power condition timer set to zero indicates that the associated power condition is disabled.

If the power condition is enabled, then the value of each timer specifies the time after command completion that the device waits before transitioning to the power condition. All enabled power condition timers run concurrently.

On command completion all timers that were stopped are initialized with the Current Timer settings values and started.

As a result of processing any command, the device may change to a different power condition.

If an enabled timer associated with a power condition lower than the power condition that the device is currently in expires, then the device transitions to the power condition associated with that timer (e.g., if the standby_z timer is set to a smaller interval than the idle_b timer, and the device is currently in the standby_z power condition, then the device remains in the Standby_z power condition when the idle_b timer expires). If the timer expiration qualifies the device to transition to more than one enabled power condition, then the device transitions to the power condition with the least power consumption.

If a command is accepted that requires a transition to Active, then the timers are stopped. If a command is accepted that does not require a transition to Active (e.g., a CHECK POWER MODE command), then the timers continues to run.

Prior to entering into any power condition that prevents accessing the media (e.g., before a hard drive stops its spindle motor during transition to the standby_z power condition) and if volatile write cache is enabled, then the device shall write all cached data to the medium for the device (e.g., as a device does in response to a flush command).

9.20.3   Interation with Resets, Commands, and other Features

On successful processing of a power cycle, the EPC enables sub command, the device:
When EPC is Enabling, the following content is executed.
  1) stop all EPC timers.
  2) copy the Saved Timer Enabled field to the Current Timer Enabled field, for all supported power conditions.
  3) copy the Saved Timer Settings field to the Current Timer Settings field, for all supported power conditions.
  4) initialize and restart all enabled EPC timers with Current values.

On successful processing of a hardware reset, a software reset, or a DEVICE RESET command, the device:
When EPC is Enabling, the following content is executed.
  1) stop all EPC timers.
  2) remain in the current power condition.
  3) initialize and restart all enabled EPC timers with Current values.

The Extended Power Conditions feature set and the Advanced Power Management feature set are mutually exclusive. All EPC subcommands, except Enable the EPC feature set, returns command aborted if the EPC feature set is disabled. If the device processes a SET FEATURES Enable APM subcommand without error and IDENTIFY DEVICE data word 120 bit 7 is set to one, then the device shall disable the EPC feature set.

During background activities, all EPC timers are stopped. On completion of the activity, any stopped EPC timers be continued from where they were paused.

9.21   Sanitize Device Feature Set

9.21.1   Overview

The Sanitize Device Feature Set allows hosts to request that devices modify the content of all user data areas in the device using sanitize operations. Sanitize operations use one of the operations defined in this sub clause to make all previously written content in the user data area of the device unable to be read. Sanitize operations affect the following:

a)   user data areas

b)   user data areas that are not currently allocated (e.g., previously allocated areas and physical sectors that have become inaccessible)

c)   user data caches

Sanitize operations render user data previously stored in caches, using any methods, unable to be read.

The Sanitize Device feature set is implemented, the following commands are supported:

a)   SANITIZE STATUS EXT

b)   SANITIZE FREEZE LOCK EXT

c)   OVERWRITE EXT

If physical sectors that have become inaccessible are not successfully sanitized, then Sanitize operations don't cause a transition to the SD3: Sanitize Operation Failed state.

Sanitize operations don't affect non-user data areas (e.g., logs, and Device SMART data structure).

Sector reallocation is able to be performed during the operation of this function. After completion of a sanitize operation, if:

a)   all physical sectors that are available to be allocated for user data have been successfully sanitized

b)   any physical areas that were not successfully sanitized were removed from use,

then:

a)   the Sanitize Device state machine transitions to SD4: Sanitize Operation Succeeded; and

b)   in subsequent SANITIZE STATUS EXT commands, set the SANITIZE OPERATION COMPLETED WITHOUT ERROR bit to one in the Normal Outputs

Conversely, if physical sectors that are available to be allocated for user data (e.g. allocated physical sectors) were not successfully sanitized, then:

a)   the Sanitize Device state machine transitions to SD3: Sanitize Operation Failed; and

b)   in subsequent SANITIZE STATUS EXT commands, return an error and set the LBA field of the Error Outputs to report the value of Sanitize Command Unsuccessful

To initiate a sanitize operation the host issues one of the following sanitize operation commands:

a)   An OVERWRITE EXT command

The sanitize operation continues after command completion of the initiating sanitize operation command. The SANITIZE STATUS EXT command to reports progress and completion.

After a device has started processing a sanitize operation, and until the device transitions to the SD0:

Sanitize Idle state, the device aborts all commands other than:

a)   IDENTIFY DEVICE command

b)   IDLE IMMEDIATE command with UNLOAD feature

c)   Request Sense Data Ext command;

d)   SANITIZE STATUS EXT command;

e)   SMART READ LOG command requesting log address E0h;

f)   READ LOG EXT command requesting one of the following log addresses:

    A)   E0h;

    B)   30h; or

    C)   10h;

g) READ LOG DMA EXT command requesting one of the following log addresses:

    A) E0h;

    B) 30h; or

    C) 10h;

h) SMART RETURN STATUS command; or

i) SET FEATURES PUIS feature set device spin-up subcommand.

If a sanitize operation is interrupted by a power-on reset, the sanitize operation continues. If the device processes a power-on reset and enters the PM5: PUIS and spin-up subcommand not supported state (see Figure 14), then the device resumes processing the sanitize operation after receiving a media access command. (The media access command reports failure because the sanitize operation does not allow media access commands. However, since the device has received a media access command, the device is spin-up.)

The SANITIZE STATUS EXT command returns information about the current sanitize operation, if any, including a percentage of completion if a sanitize operation is in progress.

An OVERWRITE EXT command that returns command completion with no error transitions the device into the SD2: Sanitize Operation state. The device remains in this state until the device has completed the sanitize operation (see *Section 6.3.1 Input Voltage*).

The SANITIZE FREEZE LOCK EXT command causes the device to transition to the SD1: Sanitize Frozen state and causes any subsequent OVERWRITE EXT command to be aborted. If the device processes a power-on reset or a hardware reset, then the device transitions from the Sanitize Frozen state to the Sanitize Idle state.

The overwrite operation fills all user data with a four byte pattern passed within the LBA field of the command. Parameters for the OVERWRITE EXT command include a count for multiple overwrites and the option to invert the four byte pattern between consecutive overwrite passes.

A software reset does not cause the SD2: Sanitize Operation state to transition to another state.

9.21.2   Sanitize Device Feature

The Sanitize Device Feature Set is a powerful data erase feature. Overwrite Ext Command supports erasure of user data.

Individual Sanitize Device commands are identified by the value specified in the FEATURE field.

The following commands are supported for this feature.

Command	COMMAND field value	FEATURE field value
SANITIZE STATUS EXT	('B4'h)	('0000'h)
OVERWRITE EXT	('B4'h)	('0014'h)
SANITIZE FREEZE LOCK EXT	('B4'h)	('0020'h)

9.21.3   Sanitize Device State Machine

Figure 14 describes the operation of the Sanitize Device state machine.

9.21.3.1   SD0: Sanitize Idle State

In SD0: Sanitize Idle state the Sanitize Device state machine is ready for a sanitize operation command or a SANITIZE FREEZE LOCK EXT command.
This state is entered when the device processes a power-on reset while in the SD1: Sanitize Freeze Lock state or the SD4: Sanitize Operation Succeeded state.
While in this state, Sanitize Device state machine does not change state if the device processes:

    a)   a hardware reset or power-on reset

    b)   a SANITIZE STATUS EXT command.

Transition SD0:SD1: If the device processes a SANITIZE FREEZE LOCK EXT command, then the device transitions to the SD1: Sanitize Frozen state.
Transition SD0:SD2: If the device successfully processes a supported sanitize operation command, then the device transitions to the SD2: Sanitize Operation state.

Figure 11   Sanitize Device State Machines
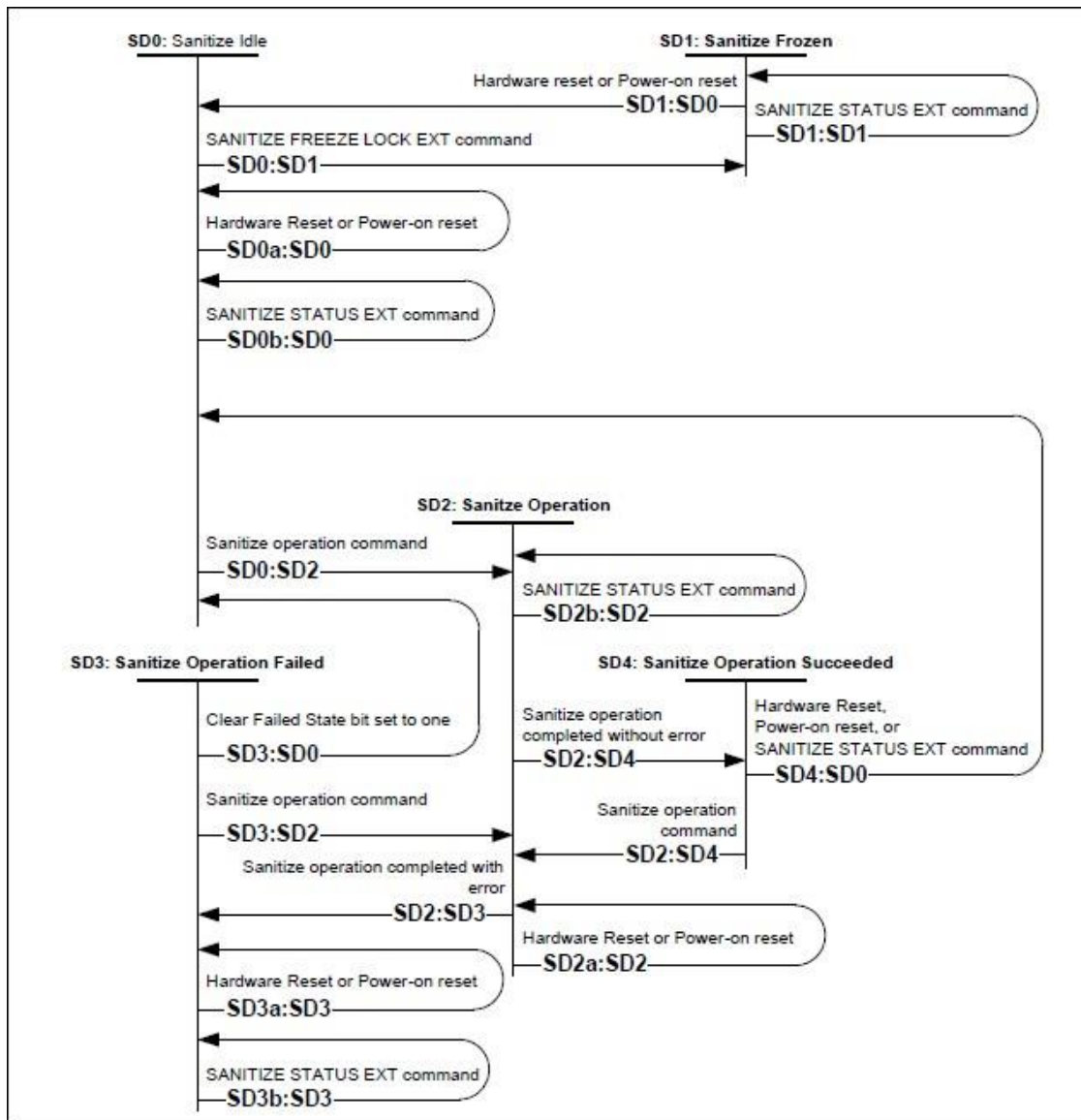
9.21.3.2   SD1: Sanitize Frozen State

In SD1: Sanitize Frozen state, the device will abort Sanitize operation commands.
While in this state, Sanitize Device state machine does not change state if the device processes a SANITIZE STATUS EXT command.
Transition SD1:SD0: If the device processes a hardware reset or a power-on reset, then the device transitions to the SD0: Sanitize Idle state.

9.21.3.3   SD1SD2: Sanitize Operation State

In the SD2: Sanitize Operation state, the device is processing a sanitize operation.
While in this state, Sanitize Device state machine does not change state if the device processes:
   a)   a hardware reset or power-on reset; and
   b)   a SANITIZE STATUS EXT command.
Transition SD2:SD3: If a sanitize operation completes with an error, then the device transitions to the SD3: Sanitize Operation Failed state.
Transition SD2:SD4: If a sanitize operation completes without an error, then the device transitions to the SD4: Sanitize Operation Succeeded state.

9.21.3.4   SD1SD3: Sanitize Operation Failed State

In the SD3: Sanitize Operation Failed state, the device has completed processing a sanitize operation without success.
While in this state, Sanitize Device state machine does not change state if the device processes:
   a)   a hardware reset or power-on reset; and
   b)   a SANITIZE STATUS EXT command with the CLEAR SANITIZE OPERATION FAILED bit cleared to zero.
Transition SD3:SD0: If
   a)   the Sanitize operation was initiated by a Sanitize operation command with the FAILURE MODE bit set to one; and
   b)   the SANITIZE STATUS EXT command has been successfully processed with the CLEAR SANITIZE OPERATION FAILED bit set to one,
then the device transitions to the SD0: Sanitize Idle state.

Transition SD3:SD2: If the device processes a supported sanitize operation command that reports command completion with no error, then the device transitions to the SD2: Sanitize Operation state.

9.21.3.5   SD4: Sanitize Operation Succeeded State

In the SD4: Sanitize Operation Succeeded state, the device has completed processing a successful sanitize operation.
Transition SD4:SD0: If the device processes
   a)   a hardware reset;
   b)   a power-on reset; or
   c)   a SANITIZE STATUS EXT command
then the device transitions to the SD0: Sanitize Idle state.

Transition SD4:SD2: If the device successfully processes a supported Sanitize operation command, then the device transitions to the SD2: Sanitize Operation state.

10   Command Protocol

The commands are grouped into different classes according to the protocols followed for command execution. The command classes with their associated protocols are defined below.

Please refer to Serial ATA Revision 3.5 about each protocol.

For all commands, the host must first check if BSY=1, and should proceed no further unless and until BSY=0. For all commands, the host must also wait for RDY=1 before proceeding.

A device must maintain either BSY=1 or DRQ=1 at all times until the command is completed. The INTRQ signal is used by the device to signal most, but not all, times when the BSY bit is changed from 1 to 0 during command execution.

A command shall only be interrupted with a COMRESET or software reset. The result of writing to the Command register while BSY=1 or DRQ=1 is unpredictable and may result in data corruption. A command should only be interrupted by a reset at times when the host thinks there may be a problem, such as a device that is no longer responding.

Interrupts are cleared when the host reads the Status Register, issues a reset, or writes to the Command Register.

10.1   PIO Data-In Commands

These commands are:
- Identify Device
- Read Buffer
- Read Log Ext
- Read Multiple
- Read Multiple Ext
- Read Sector(s)
- Read Sector(s) Ext
- SMART Read Attribute Values
- SMART Read Attribute Thresholds
- SMART Read Log Sector

Execution includes the transfer of one or more 512 byte sectors of data from the device to the host.

10.2   PIO Data-Out Commands

These commands are:
- Download Microcode
- Security Disable Password
- Security Erase Unit
- Security Set Password
- Security Unlock
- SMART Write Log Sector
- Write Buffer
- Write Log Ext
- Write Multiple
- Write Multiple Ext
- Write Multiple FUA Ext
- Write Sector(s)
- Write Sector(s) Ext

Execution includes the transfer of one or more 512 byte sectors of data from the host to the device.

10.3   Non-Data Commands

These commands are:

- Check Power Mode
- Execute Device Diagnostic
- Flush Cache
- Flush Cache Ext
- Idle
- Idle Immediate
- Initialize Device Parameters
- NCQ NON-DATA
- NOP
- Overwrite Ext
- Read Verify Sector(s)
- Read Verify Sector(s) Ext
- Recalibrate
- Sanitize Freeze Lock Ext
- Sanitize Status Ext
- Security Erase Prepare
- Security Freeze Lock
- Seek
- Set Features
- Set Multiple Mode
- Sleep
- SMART Disable Operations
- SMART Enable/Disable Attribute Autosave
- SMART Enable Operations
- SMART Execute Off-line Data Collection
- SMART Return Status
- SMART Save Attribute Values
- SMART Enable/Disable Automatic Off-Line
- Standby
- Standby Immediate
- Write Uncorrectable Ext

Execution of these commands involves no data transfer.

10.4   DMA Data-In Commands and DMA Data-Out Commands

These commands are:

- Download Microcode DMA
- Read DMA
- Read DMA Ext
- Read Log DMA Ext
- Write DMA
- Write DMA Ext
- Write DMA FUA Ext
- Write Log DMA Ext

Execution of this class of command includes the transfer of one or more blocks of data between the device and the host using DMA transfer.

10.5   First-party DMA Commands

These commands are:

- Read FPDMA Queued
- Write FPDMA Queued

Execution of this class of commands includes command queuing and the transfer of one or more blocks of data between the device and the host. The protocol is described in the section 13.6 "Native Command Queuing" of "Serial ATA Revision 3.5".

Host knowledge of I/O priority may be transmitted to the device as part of the command. There are two priority classes for NCQ command as high priority, the host is requesting a better quality of service for that command than the commands issued with normal priority.

The classes are forms of soft priority. The device may choose to complete a normal priority command before an outstanding high priority command, although preference is given to the high priority commands. The priority class is indicated in bit 7 (Priority Information) in the Sector Count register for NCQ commands (READ FPDMA QUEUED and WRITE FPDMA QUEUED). This bit can indicate either the normal priority or high priority class. If a command is marked by the host as high priority, the device attempts to provide better quality of service for the command. The device may not process all high priority requests before satisfying normal priority requests.

11   Command Descriptions

Table 70   Command Set Definitions

Protocol	Command	Code (Hex)	7	6	5	4	3	2	1	0
			\	\	\	Binary Code Bit				
3	Check Power Mode	E5	1	1	1	0	0	1	0	1
3	Check Power Mode*	98	1	0	0	1	1	0	0	0
2	Download Microcode	92	1	0	0	1	0	0	1	0
3	Execute Device Diagnostic	90	1	0	0	1	0	0	0	0
3	Flush Cache	E7	1	1	1	0	0	1	1	1
3	Flush Cache Ext	EA	1	1	1	0	1	0	1	0
1	Identify Device	EC	1	1	1	0	1	1	0	0
3	Idle	E3	1	1	1	0	0	0	1	1
3	Idle*	97	1	0	0	1	0	1	1	1
3	Idle Immediate	E1	1	1	1	0	0	0	0	1
3	Idle Immediate*	95	1	0	0	1	0	1	0	1
3	Initialize Device Parameters	91	1	0	0	1	0	0	0	1
3	NCQ NON-DATA	63	0	1	1	0	0	0	1	1
3	Overwrite Ext	B4	1	0	1	1	0	1	0	0
1	Read Buffer	E4	1	1	1	0	0	1	0	0
4	Read DMA	C8	1	1	0	0	1	0	0	0
4	Read DMA	C9	1	1	0	0	1	0	0	1
4	Read DMA Ext	25	0	0	1	0	0	1	0	1
5	Read FPDMA Queued	60	0	1	1	0	0	0	0	0
1	Read Log Ext	2F	0	0	1	0	1	1	1	1
4	Read Log DMA Ext	47	0	1	0	0	0	1	1	1
1	Read Multiple	C4	1	1	0	0	0	1	0	0
1	Read Multiple Ext	29	0	0	1	0	1	0	0	1
1	Read Sector(s)	20	0	0	1	0	0	0	0	0
1	Read Sector(s)	21	0	0	1	0	0	0	0	1
1	Read Sector(s) Ext	24	0	0	1	0	0	1	0	0
3	Read Verify Sector(s)	40	0	1	0	0	0	0	0	0
3	Read Verify Sector(s)	41	0	1	0	0	0	0	0	1
3	Read Verify Sector(s) Ext	42	0	1	0	0	0	0	1	0
3	Recalibrate	1x	0	0	0	1	-	-	-	-
3	Sanitize Freeze Lock Ext	B4	1	0	1	1	0	1	0	0
3	Sanitize Status Ext	B4	1	0	1	1	0	1	0	0
2	Security Disable Password	F6	1	1	1	1	1	0	1	0
3	Security Erase Prepare	F3	1	1	1	1	0	0	1	1
2	Security Erase Unit	F4	1	1	1	1	0	1	0	0
3	Security Freeze Lock	F5	1	1	1	1	0	1	0	1
2	Security Set Password	F1	1	1	1	1	0	0	0	1
2	Security Unlock	F2	1	1	1	1	0	0	1	0
3	Seek	7x	0	1	1	1	-	-	-	-
3	Set Features	EF	1	1	1	0	1	1	1	1
3	Set Multiple Mode	C6	1	1	0	0	0	1	1	0
3	Sleep	E6	1	1	1	0	0	1	1	0
3	Sleep*	99	1	0	0	1	1	0	0	1

Table 71 Command Set Definitions - Continued

Protocol	Command	Code (Hex)	7	6	5	4	3	2	1	0
			Binary Code Bit							
3	SMART Disable Operations	B0	1	0	1	1	0	0	0	0
3	SMART Enable/Disable Attribute Auto save	B0	1	0	1	1	0	0	0	0
3	SMART Enable Operations	B0	1	0	1	1	0	0	0	0
3	SMART Execute Off-line Data Collection	B0	1	0	1	1	0	0	0	0
1	SMART Read Attribute Values	B0	1	0	1	1	0	0	0	0
1	SMART Read Attribute Thresholds	B0	1	0	1	1	0	0	0	0
3	SMART Return Status	B0	1	0	1	1	0	0	0	0
3	SMART Save Attribute Values	B0	1	0	1	1	0	0	0	0
2	SMART Write Log Sector	B0	1	0	1	1	0	0	0	0
3	SMART Enable/Disable Automatic Off-line	B0	1	0	1	1	0	0	0	0
3	Standby	E2	1	1	1	0	0	0	1	0
3	Standby*	96	1	0	0	1	0	1	1	0
3	Standby Immediate	E0	1	1	1	0	0	0	0	0
3	Standby Immediate*	94	1	0	0	1	0	1	0	0
2	Write Buffer	E8	1	1	1	0	1	0	0	0
4	Write DMA	CA	1	1	0	0	1	0	1	0
4	Write DMA	CB	1	1	0	0	1	0	1	1
4	Write DMA Ext	35	0	0	1	1	0	1	0	1
4	Write DMA FUA Ext	3D	0	0	1	1	1	1	0	1
5	Write FPDMA Queued	61	0	1	1	0	0	0	0	1
2	Write Log Ext	3F	0	0	1	1	1	1	1	1
4	Write Log DMA Ext	57	0	1	0	1	0	1	1	1
2	Write Multiple	C5	1	1	0	0	0	1	0	1
2	Write Multiple Ext	39	0	0	1	1	1	0	0	1
2	Write Multiple FUA Ext	CE	1	1	0	0	1	1	1	0
2	Write Sector(s)	30	0	0	1	1	0	0	0	0
2	Write Sector(s)	31	0	0	1	1	0	0	0	1
2	Write Sector(s) Ext	34	0	0	1	1	0	1	0	0
3	Write Uncorrectable Ext	45	0	1	0	0	0	1	0	1

Protocol :
- 1 : PIO data IN command
- 2 : PIO data OUT command
- 3 : Non data command
- 4 : DMA command
- 5 : DMA Queued command
- + : Vendor specific command

Commands marked * are alternate command codes for previous defined commands.

Table 72 Command Set (Subcommand)

Command (Subcommand)	Command code (Hex)	Feature Register (Hex)
(SMART Function)		
SMART Read Attribute Values	B0	D0
SMART Read Attribute Thresholds	B0	D1
SMART Enable/Disable Attribute Autosave	B0	D2
SMART Save Attribute Values	B0	D3
SMART Execute Off-line Data Collection	B0	D4
SMART Read Log	B0	D5
SMART Write Log	B0	D6
SMART Enable Operations	B0	D8
SMART Disable Operations	B0	D9
SMART Return Status	B0	DA
SMART Enable/Disable Automatic Off-line	B0	DB
(Set Features)		
Enable Write Cache	EF	02
Set Transfer Mode	EF	03
Enable Advanced Power Management	EF	05
Enable Power-up in Standby Feature Set	EF	06
Power-up in Standby Feature Set Device Spin-up	EF	07
Disable read look-ahead feature	EF	55
Disable reverting to power on defaults	EF	66
Disable write cache	EF	82
Disable Advanced Power Management	EF	85
Disable Power-up in Standby Feature Set	EF	86
Enable read look-ahead feature	EF	AA
Enable reverting to power on defaults	EF	CC
(Sanitize Device Feature Set)		
Sanitize Status Ext	B4	0000
Overwrite Ext	B4	0014
Sanitize Freeze Lock Ext	B4	0020
(NCQ NON-DATA)		
Abort NCQ queue – Abort All	63	00
Abort NCQ queue – Abort Streaming	63	10
Abort NCQ queue – Abort Non-Streaming	63	20
Abort NCQ queue – Abort Selected	63	30
Deadline Handling – WDNC	63	Set:11 Clear:01
Deadline Handling – RDNC	63	Set:21 Clear:01

Tables 70 and 71 **Command Set Definitions** - show the commands that are supported by the device.

Table 72 **Command Set (Subcommand)** - shows the sub-commands that are supported by each command or feature.

The following symbols are used in the command descriptions:

Output Registers

0   Indicates that the bit must be set to 0.

1   Indicates that the bit must be set to 1.

D   The device number bit.   Indicates that the device number bit of the Device/Head Register should be specified. This bit is reserved since all Serial ATA devices behave like Device 0.

H   Head number.   Indicates that the head number part of the Device/Head Register is an output parameter and should be specified.

L   LBA mode.   Indicates the addressing mode. Zero specifies CHS mode and one does LBA addressing mode.

R   Retry. Original meaning is already obsolete, there is no difference between 0 and 1. (Using 0 is recommended for future compatibility.)

B   Option Bit. Indicates that the Option Bit of the Sector Count Register should be specified.

V   Valid. Indicates that the bit is part of an output parameter and should be specified.

X   Indicates that the hex character is not used.

-   Indicates that the bit is not used.

Input Registers

0   Indicates that the bit is always set to 0.

1   Indicates that the bit is always set to 1.

H   Head number. Indicates that the head number part of the Device/Head Register is an input parameter and will be set by the device.

V   Valid. Indicates that the bit is part of an input parameter and will be set to 0 or 1 by the device.

-   Indicates that the bit is not part of an input parameter.

The command descriptions show the contents of the Status and Error Registers after the device has completed processing the command and has interrupted the host.

Please refer to ATA interface specifications about other commands' descriptions which are not described in this SATA interface specification.   However, be careful that Serial ATA Device/Head register bit-4 (d) is different from that of Parallel ATA.   In Serial ATA, Device/Head register bit-4 is reserved for all commands.

11.1 Check Power Mode (E5h/98h)

Table 73 Check Power Mode Command (E5h/98h)

Command Block Output Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	0	0	1	0	1

Command Block Input Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below…							
Sector Count	V	V	V	V	V	V	V	V
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

The Check Power Mode command will report whether the device is spun up and the media is available for immediate access.

Input Parameters From The Device

Sector Count   The power mode code.

If the Extended Power Conditions feature set is disabled and the device is in Idle mode, Check Power Mode returns FFh by Sector Count Register, instead of returning 80h. Check Power Mode returns 0 in the Sector Count Register if the device is in Standby mode.

If the Extended Power Conditions feature set is enabled, the command returns power condition. idle_a condition is 81h, idle_b condition is 82h, idle_c condition is 83h, standby_y condition is 01h, standby_z condition is 00h.

11.2 Download Microcode (92h)

Table 74 Download Microcode Command (92h)

Command Block Output Registers										Command Block Input Registers									
Register	7	6	5	4	3	2	1	0		Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-		Data	-	-	-	-	-	-	-	-
Feature	SUBCOMMAND(00-07)									Error	…See Below…							
Sector Count	SECTOR_COUNT(00-07)									Sector Count	-	-	-	-	-	-	-	-
Sector Number	SECTOR_COUNT(08-15)									Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	BUFFER_OFFSET(00-07)									Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	BUFFER_OFFSET(08-15)									Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	D	-	-	-	-		Device/Head	-	-	-	-	-	-	-	-
Command	1	0	0	1	0	0	1	0		Status	…See Below…							

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	0	0	V	0	0		0	1	0	1	0	0	-	V

Output Parameters To The Device

Feature   Subcommand code.

    03h : Download and save microcode with offsets.

    07h : Download and save microcode.

    0Eh : Download with offsets and save microcode.

    0Fh : Activate download microcode.

    Other values are reserved.

Sector Count   Lower byte of 16-bit sector count value to transfer from the host.

Sector Number   Higher byte of 16-bit sector count value to transfer from the host.

Cylinder   Buffer offset (only used for Feature = 03h)

This command enables the host to alter the device's microcode. The data transferred using the DOWNLOAD MICROCODE commands is vendor specific.

The Download and save microcode with offsets subcommand(03h) transfers the updated microcode data in one or more DOWNLOAD MICROCODE commands. This subcommand downloads data containing a segment of the updated microcode data. On normal command completion, the COUNT field may contain additional indicators.
If the final segment has been downloaded, the device validates the downloaded updated microcode. If the validation is successful, the downloaded updated microcode is saved to non-volatile storage and is activated.
After transferring a segment where the value of the BUFFER OFFSET field is cleared to zero, if the device begins to process a command that is not a DOWNLOAD MICROCODE command, then the device:
1) may discard any updated microcode data that has not been saved; and
2) shall continue to process the new command.

The Download and save microcode subcommand(07h) transfers the updated microcode data in one DOWNLOAD MICROCODE command.

After the updated microcode data has been downloaded:
1) the device shall save the updated microcode data;
2) the device shall activate the updated microcode data; and

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3) if command completion has not previously been returned, then the device shall return command completion.

The Download with offsets and save microcode subcommand(0Eh) transfers the updated microcode data in one or more DOWNLOAD MICROCODE commands. On normal command completion, the COUNT field may contain additional indicators.

If the final segment has been downloaded, the device validates the downloaded updated microcode. If the validation is successful, the downloaded updated microcode is saved to non-volatile storage and becomes the deferred microcode. The deferred microcode data is activated as a result of processing the next power on reset or processing an Activate downloaded microcode subcommand.

The processing of commands other than the DOWNLOAD MICROCODE command shall not affect any:
1) updated microcode; and
2) saved microcode.

The Activate downloaded microcode subcommand(0Fh) shall activate deferred microcode data that had been previously downloaded and saved by the Download with offsets and save microcode subcommand.

11.3 Download Microcode DMA (93h)

Table 75 Download Microcode DMA Command (93h)

Command Block Output Registers	7	6	5	4	3	2	1	0	Command Block Input Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0	Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-	Data	-	-	-	-	-	-	-	-
Feature	SUBCOMMAND(00-07)								Error	…See Below…							
Sector Count	SECTOR_COUNT(00-07)								Sector Count	-	-	-	-	-	-	-	-
Sector Number	SECTOR_COUNT(08-15)								Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	BUFFER_OFFSET(00-07)								Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	BUFFER_OFFSET(08-15)								Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	D	-	-	-	-	Device/Head	-	-	-	-	-	-	-	-
Command	1	0	0	1	0	0	1	1	Status	…See Below…							

Error Register								Status Register							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN	BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	0	0	V	0	0	0	1	0	1	0	0	-	V

Output Parameters To The Device

Feature   Subcommand code.

          03h : Download and save microcode with offsets.

          07h : Download and save microcode.

          0Eh : Download with offsets and save microcode.

          0Fh : Activate download microcode.

          Other values are reserved.

Sector Count   Lower byte of 16-bit sector count value to transfer from the host.

Sector Number   Higher byte of 16-bit sector count value to transfer from the host.

Cylinder   Buffer offset (only used for Feature = 03h)

This command enables the host to alter the device's microcode. The data transferred using the DOWNLOAD MICROCODE DMA commands is vendor specific.

The Download and save microcode with offsets subcommand(03h) transfers the updated microcode data in one or more DOWNLOAD MICROCODE commands. This subcommand downloads data containing a segment of the updated microcode data. On normal command completion, the COUNT field may contain additional indicators.
If the final segment has been downloaded, the device validates the downloaded updated microcode. If the validation is successful, the downloaded updated microcode is saved to non-volatile storage and is activated.
After transferring a segment where the value of the BUFFER OFFSET field is cleared to zero, if the device begins to process a command that is not a DOWNLOAD MICROCODE command, then the device:

    1) may discard any updated microcode data that has not been saved; and

    2) shall continue to process the new command.

The Download and save microcode subcommand(07h) transfers the updated microcode data in one DOWNLOAD MICROCODE command.

After the updated microcode data has been downloaded:
1) the device shall save the updated microcode data;

2) the device shall activate the updated microcode data; and

3) if command completion has not previously been returned, then the device shall return command completion.

The Download with offsets and save microcode subcommand(0Eh) transfers the updated microcode data in one or more DOWNLOAD MICROCODE commands. On normal command completion, the COUNT field may contain additional indicators.

If the final segment has been downloaded, the device validates the downloaded updated microcode. If the validation is successful, the downloaded updated microcode is saved to non-volatile storage and becomes the deferred microcode. The deferred microcode data is activated as a result of processing the next power on reset or processing an Activate downloaded microcode subcommand.

The processing of commands other than the DOWNLOAD MICROCODE command shall not affect any:
1) updated microcode; and
2) saved microcode.

The Activate downloaded microcode subcommand(0Fh) shall activate deferred microcode data that had been previously downloaded and saved by the Download with offsets and save microcode subcommand.

11.4   Execute Device Diagnostic (90h)

Table 76   Execute Device Diagnostic Command (90h)

Command Block Output Registers										Command Block Input Registers									
Register		7	6	5	4	3	2	1	0	Register		7	6	5	4	3	2	1	0
Data		-	-	-	-	-	-	-	-	Data		-	-	-	-	-	-	-	-
Feature		-	-	-	-	-	-	-	-	Error				…See Below…					
Sector Count		-	-	-	-	-	-	-	-	Sector Count		-	-	-	-	-	-	-	-
Sector Number		-	-	-	-	-	-	-	-	Sector Number		-	-	-	-	-	-	-	-
Cylinder Low		-	-	-	-	-	-	-	-	Cylinder Low		-	-	-	-	-	-	-	-
Cylinder High		-	-	-	-	-	-	-	-	Cylinder High		-	-	-	-	-	-	-	-
Device/Head		1	-	1	-	-	-	-	-	Device/Head		-	-	-	-	-	-	-	-
Command		1	0	0	1	0	0	0	0	Status				…See Below…					

Error Register
Diagnostic Code

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	0

The Execute Device Diagnostic command performs the internal diagnostic tests implemented by the device. The results of the test are stored in the Error Register.

The normal Error Register bit definitions do not apply to this command. Instead, the register contains a diagnostic code. See Table 31 Diagnostic Codes in *Section 9.1.1 "Register Initialization"* for its definition.

11.5 Flush Cache (E7h)

This command causes the device to complete writing data from its cache. The device returns good status after data in the write cache is written to disk media.

Table 77 Flush Cache Command (E7h)

Command Block Output Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	0	0	1	1	1

Command Block Input Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below…							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

This command causes the device to complete writing data from its cache.

The device returns good status after data in the write cache is written to disk media.

11.6   Flush Cache Ext (EAh)

This command causes the device to complete writing data from its cache. The device returns good status after data in the write cache is written to disk media.

Table 78   Flush Cache Ext Command (EAh)

Command Block Output Registers		7	6	5	4	3	2	1	0
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Feature	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Sector Count	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Sector Number	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Cylinder Low	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Cylinder High	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Device/Head		-	-	-	D	-	-	-	-
Command		1	1	1	0	1	0	1	0

Command Block Input Registers		7	6	5	4	3	2	1	0
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Error		…See Below…							
Sector Count	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Sector Number	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Cylinder Low	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Cylinder High	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Device/Head		-	-	-	-	-	-	-	-
Status		…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

This command causes the device to complete writing data from its cache.

The device returns good status after data in the write cache is written to disk media.

11.7   Identify Device (ECh)

The Identify Device command requests the device to transfer configuration information to the host. The device will transfer a sector to the host containing the information described in the following pages.

Table 79   Identify Device Command (ECh)

Command Block Output Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	0	1	1	0	0

Command Block Input Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below…							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

The Identify Device command requests the device to transfer configuration information to the host. The device will transfer a sector to the host containing the information described in the following pages.

Table 80   Identify Device Information

Word	Content		Description
00	045AH or 045EH		Drive classification, bit assignments: 15 (=0): 1=ATAPI device, 0=ATA device 14-8 : retired 7 (=0): 1=removable cartridge device 6 (=1): 1=fixed device 5-3 : retired 2 (=0): Response incomplete 1 : retired 0 (=0): Reserved
01	xxxxH		Number of cylinders in default translate mode
02	C837H		Specific Configuration 37C8H: Need Set Feature for spin-up after power-up Identify Device is incomplete 738CH: Need Set Feature for spin-up after power-up Identify Device is complete 8C73H: No Need Set Feature for spin-up after power-up Identify Device is incomplete C837H: No Need Set Feature for spin-up after power-up Identify Device is complete
03	00xxH		Number of heads in default translate mode
04	0	*	Reserved
05	0	*	Reserved
06	003FH		Number of sectors per track in default translate mode
07	0000H	*	Number of bytes of sector gap
08	0000H	*	Number of bytes in sync field
09	0000H	*	Reserved
10-19	XXXX		Serial number in ASCII (0 = not specified)
20	0000H	*	Controller type: 0003: dual ported, multiple sector buffer with look-ahead read
21	0000H	*	Buffer size in 512-byte increments. In case of 64MB buffer, it is set to 0x0000.
22	0000H	*	Reserved
23-26	XXXX		Microcode version in ASCII
27-46	XXXX		Model number in ASCII
47	8010H		15-8 : 80h 7-0 : Maximum number of sectors that can be transferred per interrupt on Read and Write Multiple commands
48	400XH		Trusted Computing feature set options 15 (=0) : Shall be cleared to zero 14 (=1) : Shall be set to one 13-1 (=0) : Reserved for the Trusted Computing Group 0 (=0 or 1) : 0=Trusted Computing feature set is not supported 1=Trusted Computing feature set is supported

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Table 81   Identify Device Information - Continued

Word	Content		Description
49	xF00H		Capabilities, bit assignments: 15-14 (=0) Reserved 13 Standby timer (=1) values as specified in ATA standard are supported (=0) values are vendor specific 12 (=0) Reserved 11 (=1) IORDY Supported 10 (=1) IORDY can be disabled 9 (=1) LBA supported 8 (=1) DMA supported 7- 0 (=0) Reserved
50	4000H		Capabilities, bit assignments: 15-14 (=01) word 50 is valid 13- 1 (=0) Reserved 0 Minimum value of Standby timer (=0) less than 5 minutes
51	0200H		PIO data transfer cycle timing mode
52	0200H	*	DMA data transfer cycle timing mode Refer Word 62 and 63
53	0006H		Validity flag of the word 15- 8 (=0): Free-fall Control Sensitivity 00h = Vendor's recommended setting 7-3 (=0): Reserved 2 (=1): 1=Word 88 is Valid 1 (=1): 1=Word 64-70 are Valid 0 (=1): 1=Word 54-58 are Valid
54	xxxxH		Number of current cylinders
55	xxxxH		Number of current heads
56	xxxxH		Number of current sectors per track
57-58	xxxxH		Current capacity in sectors Word 57 specifies the low word of the capacity
59	xxxxH		Sanitize capabilities and Current Multiple setting. Bit assignments 15 (=0) The BLOCK ERASE EXT command is supported 14 (=1) The OVERWRITE EXT command is supported 12 (=1) The Sanitize Device Feature Set is supported 11(=1) The commands allowed during a sanitize operation 10-9 (=0) Reserved 8 1= Multiple Sector Setting is Valid 7-0 xxh = Current setting for number of sectors
60-61	xxxxH		Total Number of User Addressable Sectors Word 60 specifies the low word of the number FFFFFFFh=The 48-bit native max address is greater than 268,435,455
62	0000H		Reserved
63	xx07H		Multiword DMA Transfer Capability 15- 8 Multi word DMA transfer mode active 7-0 (=7) Multi word DMA transfer modes supported (support mode 0,1 and 2)
64	0003H		Flow Control PIO Transfer Modes Supported 15-8 (=0) Reserved 7-0 (=3) Advanced PIO Transfer Modes Supported '11' = PIO Mode 3 and 4 Supported

Table 82 Identify Device Information -Continued

Word	Content	Description
65	0078H	Minimum Multiword DMA Transfer Cycle Time Per Word 15-0 (=78) Cycle time in nanoseconds (120ns, 16.6MB/s)
66	0078H	Manufacturer's Recommended Multiword DMA Transfer Cycle Time 15-0 (=78) Cycle time in nanoseconds (120ns, 16.6MB/s)
67	0078H	Minimum PIO Transfer Cycle Time Without Flow Control 15-0 (=78) Cycle time in nanoseconds (120ns, 16.6MB/s)
68	0078H	Minimum PIO Transfer Cycle Time With IORDY Flow Control 15- 0 (=78) Cycle time in nanoseconds (120ns, 16.6MB/s)
69	0D08H	Additional Supported 11 (=1) READ BUFFER DMA command is supported 10 (=1) WRITE BUFFER DMA command is supported 8 (=1) DOWNLOAD MICROCODE DMA is supported 4 (=x) Encryption All User Data 3 (=1) Extended Number of User Addressable Sectors is supported
70-74	0000H	Reserved
75	001FH	Queue depth 15-5 (=0) Reserved 4-0 (=1F) Maximum queued depth – 1
76	9F0EH	SATA capabilities 15 (=1) READ LOG DMA EXT command is supported 14-13 (=0) Reserved 12 (=1) High Priority command (Please see 6.5 First-party DMA commands) 11 (=0) Unload while NCQ commands are outstanding is supported 10 (=1) Phy event counters 9 (=1) Receipt of host-initiated interface power management requests 8 (=1) Native Command Queuing supported 7-4 (=0) Reserved 3 (=x) SATA Gen-3 speed (6.0Gbps) supported 2 (=x) SATA Gen-2 speed (3.0Gbps) supported 1 (=1) SATA Gen-1 speed (1.5Gbps) supported 0 (=0) Reserved
77	007xH	15-8 (=0) Reserved 7 (=0) DevSleep_to_ReducedPwrState 6 (=1) Supports RECEIVE FPDMA QUEUED and SEND FPDMA QUEUED 5 (=1) Supports NCQ NON-DATA Command 4 (=1) Supports NCQ Streaming 3-1 (=011) Current negotiated SATA speed Gen-3 speed of 6.0Gbps (=010) Current negotiated SATA speed Gen-2 speed of 3.0Gbps (=001) Current negotiated SATA speed Gen-1 speed of 1.5Gbps 0(=0) Reserved

Table 83 Identify device information -Continued

Word	Content	Description
78	08CCH	SATA supported features
		15-12 (=0) Reserved
		11 (=1) Rebuild Assist
		10 (=1) Device Initiated Interface Power Management Software Settings
		9-8 (=0) Reserved
		7 (=1) NCQ Autosense
		6 (=1) Software setting preservation
		5 (=0) Reserved
		4 (=1) In-order data delivery
		3 (=1) Device initiated interface power management
		2 (=1) DMA Setup Auto-Activate optimization
		1 (=1) Non-zero buffer offset in DMA Setup FIS
		0 (=0) Reserved
79	0040H	SATA enabled features
		15-12 (=0) Reserved
		11 (=0) Rebuild Assist enabled
		10-9 (=0) Reserved
		8-7 (=0) Reserved
		6 (=1) Software setting preservation
		5 (=0) Reserved
		4 (=0) In-order data delivery
		3 (=0) Device initiated interface power management
		2 (=0) DMA Setup Auto-Activate optimization
		1 (=0) Non-zero buffer offset in DMA Setup FIS
		0 (=0) Reserved
80	0FFEH	Major version number
		15-0 (=3FCh) ATA-2, ATA-3, ATA/ATAPI-4, ATA/ATAPI-5, ATA/ATAPI-6. ATA/ATAPI-7, ATA8-ACS, ACS-2 and ACS-3
81	009CH	Minor version number
		15-0(=29h) ATA8-ACS Revision 4
82	706BH	Command
		15 (=0) Reserved
		14 (=1) NOP command
		13 (=1) READ BUFFER command
		12 (=1) WRITE BUFFER command
		11 (=0) Reserved
		10 (=1) Host Protected Area Feature Set
		9 (=0) DEVICE RESET command
		8 (=0) SERVICE interrupt
		7 (=0) Release interrupt
		6 (=1) LOOK AHEAD
		5 (=1) WRITE CACHE
		4 (=0) PACKET Command feature set
		3 (=1) Power management feature set
		2 (=0) Removable feature set
		1 (=1) Security feature set
		0 (=1) SMART feature Set

Table 84   Identify device information -Continued

Word	Content	Description
83	7479H	Command set supported 15-14 (=01) Word 83 is valid 13 (=1) FLUSH CACHE EXT command supported 12 (=1) FLUSH CACHE command supported 11 (=1) Device Configuration Overlay command supported 10 (=1) 48-bit Address feature set supported 9 (=0) Reserved 8 (=1) SET Max Security extension 7 (=0) Set Features Address Offset feature mode 6 (=1) SET FEATURES subcommand required to spin-up after power-up 5 (=1) Power-Up In Standby feature set supported 4 (=0) Removable Media Status Notification feature 3 (=1) Advanced Power Management feature set 2 (=0) CFA feature set 1 (=0) READ/WRITE DMA QUEUED 0 (=1) DOWNLOAD MICROCODE command
84	6163H	Command set/feature supported extension 15-14 (=01) Word 84 is valid 13 (=0) IDLE IMMEDIATE with UNLOAD FEATURE supported 12-11 (=0) Reserved 10 (=x) URG bit supported for WRITE STREAM Ext 9 (=x) URG bit supported for READ STREAM Ext 8 (=1) World wide name supported 7 (=0) WRITE DMA QUEUED FUA EXT command supported 6 (=1) WRITE DMA FUA EXT and WRITE MULTIPLE FUA EXT commands supported 5 (=1) General Purpose Logging feature set supported 4 (=x) Streaming feature set supported 3 (=0) Media Card Pass Through Command feature set supported 2 (=0) Media serial number supported 1 (=1) SMART self-test supported 0 (=1) SMART error logging supported
85	xxxxH	Command set/feature enabled 15 Reserved 14 NOP command 13 READ BUFFER command 12 WRITE BUFFER command 11 Reserved 10 Host Protected Area feature set 9 DEVICE RESET command 8 SERVICE interrupt 7 RELEASE interrupt 6 LOOK AHEAD 5 WRITE CACHE 4 PACKET Command feature set 3 Power management feature set 2 Removable media feature set 1 Security feature set 0 SMART feature set

-

Table 85   Identify device information -Continued

Word	Content	Description
86	xxxxH	Command set/feature enabled
		15 Words 120:119 are valid.
		14 Reserved
		13 FLUSH CACHE EXT command supported
		12 FLUSH CACHE command supported
		11 Device Configuration Overlay command enabled
		10 48-bit Address features set supported
		9 Reserved
		8 Set Max Security extensions enabled
		7 Set Features Address Offset mode
		6 Set Features subcommand required to spin-up after power-up
		5 Power-Up In Standby feature set enabled
		4 Removable Media Status Notification feature
		3 Advanced Power Management Feature set
		2 CFA Feature set
		1 READ/WRITE DMA QUEUED
		0 DOWNLOAD MICROCODE command
87	6163H	Command set/feature default
		15-14 (=01) Word 87 is valid
		13 (=0) IDLE IMMEDIATE with UNLOAD FEATURE supported
		12-11 (=0) Reserved
		10 (=x) URG bit supported for WRITE STREAM Ext
		9 (=x) URG bit supported for READ STREAM Ext
		8 (=1) World wide name supported
		7 (=0) WRITE DMA QUEUED FUA EXT command supported
		6 (=1) WRITE DMA FUA EXT and WRITE MULTIPLE FUA EXT commands supported
		5 (=1) General Purpose Logging feature set supported
		4 (=x) Valid CONFIGURE STREAM command has been executed
		3 (=0) Media Card Pass Through Command feature set enabled
		2 (=0) Media serial number is valid
		1 (=1) SMART self-test supported
		0 (=1) SMART error logging supported

Table 86   Identify device information -Continued

Word	Content	Description
88	xx7FH	Ultra DMA Transfer modes 15- 8 (=xx) Current active Ultra DMA transfer mode 15 Reserved (=0) 14 Mode 6 1 = Active 0 = Not Active 13 Mode 5 1 = Active 0 = Not Active 12 Mode 4 1 = Active 0 = Not Active 11 Mode 3 1 = Active 0 = Not Active 10 Mode 2 1 = Active 0 = Not Active 9 Mode 1 1 = Active 0 = Not Active 8 Mode 0 1 = Active 0 = Not Active 7- 0 (=7F) Ultra DMA Transfer mode supported 7 Reserved (=0) 6 Mode 6 1 = Support 5 Mode 5 1 = Support 4 Mode 4 1 = Support 3 Mode 3 1 = Support 2 Mode 2 1 = Support 1 Mode 1 1 = Support 0 Mode 0 1 = Support
89	xxxxH	15 1=Extended Time is reported in bits 14:0 0=Time is reported in bits 7:0 If bit 15 is set to one 14:0 Time required for security erase unit completion Time= value(xxxxh)*2 [minutes] If bit 15 is set to zero 14:8 Reserved 7:0 Time required for security erase unit completion Time= value(xxxxh)*2 [minutes]
90	xxxxH	15 1=Extended Time is reported in bits 14:0 0=Time is reported in bits 7:0 If bit 15 is set to one 14:0 Time required for Enhanced security erase completion If bit 15 is set to zero 14:8 Reserved 7:0 Time required for Enhanced security erase completion
91	00FEH	Current Advanced power management value
92	FFFEH	Current Password Revision Code
93	0000H	COMRESET result
94	0000H	Reserved
95	xxxxH	Stream Minimum Request Size Number of sectors that provides optimum performance in streaming environment. This number shall be a power of two, with a minimum of eight sectors (4096 bytes). The starting LBA value for each streaming command should be evenly divisible by this request size.
96	xxxxH	Streaming Transfer Time – DMA The worst-case sustainable transfer time per sector for the device is calculated as follows: Streaming Transfer Time = (word 96) * (words(99:98) / 65536) If the Streaming Feature set is not supported by the device, the content of word 96 shall be zero.

Table 87   Identify device information -Continued

Word	Content	Description
97	xxxxH	Streaming Access Latency – DMA and PIO The worst-case access latency of the device for a streaming command is calculated as follows: Access Latency = (word 97) * (words(99:98) / 256) If the Streaming Feature set is not supported by the device, the content of word 97 shall be zero.
98	xxxxH	Streaming Performance Granularity
99	xxxxH	Streaming Performance Granularity
100-103	xxxxH	Total Number of User Addressable Logical Sectors for 48-bit commands
104	xxxxH	Streaming Transfer Time – PIO The worst-case sustainable transfer time per sector for the device is calculated as follows: Streaming Transfer Time = (word 104) * (words(99:98) / 65536) If the Streaming Feature set is not supported by the device, the content of word 104 shall be zero.
105	000AH	Reserved
106	6003H	Physical sector size / logical sector size 15 Shall be cleared to zero 14 Shall be set to one. 13 0=Device does not have multiple logical sectors per physical sector 12 0=Device logical sector is 256 words 11-4 Reserved 3-0 0=2^0 logical sectors per physical sector
107	0000H	Inter-seek delay for ISO-7779 acoustic testing in microseconds
108-111	xxxxH	World wide name the optional value of the world wide name for the device
112-116	0000H	Reserved
117-118	xxxxH	Logical Sector Size (Dword)
119	42DCH	Supported settings (Continued from word 84:82) 15 Shall be cleared to zero 14 Shall be set to one. 13-8 Reserved 7 1=Extended Power Conditions feature set is supported 6 1=Sense data is supported 5 0=Free-fall Control feature set is not supported 4 1=The segmented feature for download microcode is supported. 3 1=The READ/ WRITE LOG DMA EXT commands are supported. 2 1=Write Uncorrectable is supported. 1 0=Write-Read-Verify feature set is not supported 0 Reserved
120	401CH	Command set/feature enabled/supported. (Continued from word 87:85) 15 Shall be cleared to zero 14 Shall be set to one. 13-8 Reserved 7 1=Extended Power Conditions feature set is enabled 6 0=Sense data is disabled 5 0=Free-fall Control feature set is disabled 4 1=The segmented feature for download microcode is supported. 3 1=The READ/ WRITE LOG DMA EXT commands are supported. 2 1=Write Uncorrectable is supported. 1 0=Write-Read-Verify feature set is not enabled 0 Reserved

Table 88   Identify device information -Continued

Word	Content		Description
121-126	0000H		Reserved
127	0000H		Removable Media Status Notification feature set 0000H=Not supported
128	xxxxH		Security status. Bit assignments 15-9 Reserved 8 Security Level 1= Maximum, 0= High 7-6 Reserved 5 Enhanced erase 1= Support 4 Expired 1= Expired 3 Freeze 1= Frozen 2 Lock 1= Locked 1 Enabled/Disable 1= Enable 0 Capability 1= Support
129	xxxxH	*	Current Set Feature Option. Bit assignments 15-4 Reserved 3 Auto reassign enabled 1= Enable 2 Reverting enabled 1= Enable 1 Read Look-ahead enabled 1= Enable 0 Write Cache enabled 1= Enable
130-159	xxxxH	*	Reserved
160-167	0000H		Reserved
168	0002H		15-4 Reserved 3-0 Device Nominal Form Factor 02H shows 3.5inch nominal form factor
169-175	0000H		Reserved
176-205	0000H		Current media serial number (0000H=Not supported)
206	003DH		SCT Command set support 15-12 Vendor specific 11-6 Reserved 5 Action Code 5 (SCT Data Table) 1= Support 4 Action Code 4 (Features Control) 1= Support 3 Action Code 3 (Error Recovery Control) 1= Support 2 Action Code 2 (SCT Write Same) 1= Support 1 Action Code 1 (Long Sector Access) 0= Not Support 0 SCT Feature Set (includes SCT status) 1= Support

Note. The '*' mark in 'Content' field indicates the use of those parameters are vendor specific.

Table 89   Identify device information -Continued

Word	Content	Description
207-208	0000H	Reserved
209	4000H or 0000H	Alignment of logical blocks within a physical block (This word is valid if bit 13 of word 106 is set to one.) 15 Shall be cleared to zero 14 Shall be set to one 13-0 Logical sector offset within the first physical sector where the first logical sector is placed
210-211	0000H	Write-Read-Verify Sector Count Mode 3 (Dword) 0000H=Not supported
212-213	0000H	Write-Read-Verify Sector Count Mode 2 (Dword) 0000H=Not supported
214	0000H	NV Cache Capabilities 0000H=Not supported
215-216	0000H	NV Cache Size in Logical Blocks (Dword)
217	1C20H	Nominal media rotation rate (=7200rpm)
218	0000H	Reserved
219	0000H	NV Cache Options 0000H=Not supported
220	0000H	15-8 (=0) Reserved 7-0 (=0) Write-Read-Verify feature set current mode(not supported)
221	0000H	Reserved
222	10FEH	Transport major version number 15-12 (=1) Transport Type (1= Serial) 11-8 (=0) Reserved 7 (=1) SATA Rev 3.2 6 (=1) SATA Rev 3.1 5 (=1) SATA Rev 3.0 4 (=1) SATA Rev 2.6 3 (=1) SATA Rev 2.5 2 (=1) SATA II: Extensions 1 (=1) SATA 1.0a 0 (=1) ATA8-AST
223	0021H	Transport minor version number (ATA8-AST T13 Project D1697 Revision 0b)
224-229	0000H	Reserved
230-233	xxxxH	Extended Number of User Addressable Sectors
234	0008H	Minimum number of 512-byte data blocks per DOWNLOAD MICROCODE command for mode 3
235	0000H	Maximum number of 512-byte data blocks per DOWNLOAD MICROCODE command for mode 3
236-254	0000H	Reserved
255	xxA5H	15-8 Checksum. This value is the two's complement of the sum of all bytes in byte 0 through 510 7-0 (A5) Signature

11.8   Idle (E3h/97h)

The Idle command causes the device to enter Idle mode immediately and set auto power down timeout parameter (standby timer). And then the timer starts counting down.

When the Idle mode is entered, the device is spun up to operating speed. If the device is already spinning, the spin up sequence is not executed.

During Idle mode the device is spinning and ready to respond to host commands immediately.

Table 90   Idle Command (E3h/97h)

Command Block Output Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	0	0	0	1	1

Command Block Input Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Output Parameters To The Device

Sector Count   Timeout Parameter.   If zero, then the automatic power down sequence is disabled. If non-zero, then the automatic power down sequence is enabled, and the timeout interval is shown below:

Value	Description
0	Timer disabled
1-240	Value * 5
241-251	(Value-240) * 30 minutes
252	21 minutes
253	8 hours
254	Aborted
255	21 minutes 15 seconds

When the automatic power down sequence is enabled, the drive will enter Standby mode automatically if the timeout interval expires with no drive access from the host. The timeout interval will be reinitialized if there is a drive access before the timeout interval expires.

11.9   Idle Immediate (E1h/95h)

The Idle Immediate command causes the device to enter Idle mode.

The device is spun up to operating speed. If the device is already spinning, the spin up sequence is not executed.

During Idle mode the device is spinning and ready to respond to host commands immediately.

The Idle Immediate command will not affect to auto power down timeout parameter.

Table 91   Idle Immediate Command (E1h/95h)

Command Block Output Registers	7	6	5	4	3	2	1	0	Command Block Input Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0	Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-	Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-	Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-	Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-	Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-	Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-	Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-	Device/Head	-	-	-	-	-	-	-	-
Command	1	1	1	0	0	0	0	1	Status	...See Below...							

Error Register								Status Register							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN	BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	0	0	V	0	0	0	V	0	V	-	0	-	V

11.10   Initialize Device Parameters (91h)

The Initialize Device Parameters command enables the host to set the number of sectors per track and the number of heads minus 1, per cylinder. Words 54-58 in Identify Device Information reflect these parameters.

The parameters remain in effect until following events:
- Another Initialize Device Parameters command is received.
- The device is powered off.
- Soft reset occurs and the Set Feature option of CCh is set instead of 66h.

Table 92   Initialize Device Parameters Command (91h)

Command Block Output Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	H	H	H	H
Command	1	0	0	1	0	0	0	1

Command Block Input Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

Output Parameters To The Device

Sector Count   The number of sectors per track. 0 does not mean there are 256 sectors per track, but there is no sector per track.

H   The number of heads minus 1 per cylinder. The minimum is 0 and the maximum is 15.

Note:
The following conditions needs to be satisfied to avoid invalid number of cylinders beyond FFFFh.
(Total number of user addressable sectors)/((Sector Count)*(H+1)) = < FFFFh

The total number of user addressable sectors is described in Identify Device command.

11.11 NCQ NON-DATA (63h)

Table 93 defines the NCQ NON-DATA subcommands. See the referenced sections for additional information in this table.

The output from the host to the device, the command acceptance outputs for this command, the normal outputs for this command and the error outputs for this command are subcommand specific. See 11.15.1 Abort NCQ Queue Subcommand (0h) and 11.15.2 Deadline handling Subcommand (1h).

Table 93   NCQ NON-DATA command (63h)

Command Block Output Registers		7	6	5	4	3	2	1	0
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Feature	Current	V	V	V	V	V	V	V	V
	Previous	-	-	-	-	-	-	-	-
Sector Count	Current	V	V	V	V	V	-	-	-
	Previous	V	V	-	-	-	-	-	-
Sector Number	Current	V	V	V	V	V	-	-	-
	Previous	-	-	-	-	-	-	-	-
Cylinder Low	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Cylinder High	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Device/Head		-	1	-	0	-	-	-	-
Command		0	1	1	0	0	0	1	1

Command Block Input Registers		7	6	5	4	3	2	1	0
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Error				...See Below...					
Sector Count	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Sector Number	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Cylinder Low	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Cylinder High	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Device/Head		-	-	-	-	-	-	-	-
Status				…See Below…					

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
V	V	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

11.11.1 Abort NCQ Queue Subcommand (0h)

Table 94 Abort NCQ Queue Subcommand (0h)

Command Block Output Registers		7	6	5	4	3	2	1	0
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Feature	Current	V	V	V	V	0	0	0	0
	Previous	-	-	-	-	-	-	-	-
Sector Count	Current	V	V	V	V	V	-	-	-
	Previous	-	-	-	-	-	-	-	-
Sector Number	Current	V	V	V	V	V	-	-	-
	Previous	-	-	-	-	-	-	-	-
Cylinder Low	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Cylinder High	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Device/Head		-	1	-	0	-	-	-	-
Command		0	1	1	0	0	0	1	1

Command Block Input Registers		7	6	5	4	3	2	1	0
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Error				...See Below...					
Sector Count	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Sector Number	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Cylinder Low	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Cylinder High	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Device/Head		-	-	-	-	-	-	-	-
Status				…See Below…					

Error Register

7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
V	V	0	V	0	V	0	0

Status Register

7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Normal Outputs

If a supported Abort Type parameter is specified, then the device indicates success, even if the command results in no commands being aborted.

When an Abort NCQ Queue command completes successfully, a Set Device Bits FIS is sent to the host to complete the Abort subcommand and commands that were aborted as a consequence of the Abort subcommand by setting the ACT bits for those commands to one. This SDB FIS may also indicate other completed commands.

Error Outputs

The device returns command aborted if:

a) NCQ is disabled and an Abort NCQ Queue command is issued to the device;

b) the value of the TTAG field equals the value of the TAG field;

c) the value of the TTAG field is an invalid TAG number; or

d) an unsupported Abort type parameter is specified.

Output Parameters To The Device

Feature Current

Subcommand (bits 3-0)	When bits(3:0) is 0h, Abort NCQ Queue Abort Subcommand.
Subcommand Specific (bits 7-4)	Abort Type, bit(7:4), describes the action requested. The NCQ NON-DATA Log (see 9.17.4.3 Read Log Ext Log Page 12h) provides a list of abort types supported by the device. The value of Abort type are defined in the below the table.

Feature Previous

Sector Count Current

TAG (bits 7-3)	The TAG value is assigned to be different from all other queued commands. The value does not exceed the maximum queue depth specified by the Word 75 of the Identify Device information.

Sector Count Previous

Sector Number Current

TTAG (bits 7-3)	The TTAG field contains the value of the TAG of the outstanding command that is requested to be aborted. The TTAG value is only valid when the Abort Type field is set to 3h (Abort Selected). TTAG does not exceed the value specified in IDENTIFY DEVICE word 75.

Cylinder Low Current

Cylinder Low Previous

Cylinder High Current

Cylinder High Previous

Device/Head

Input Parameters From The Device

Sector Number (HOB=0)

Sector Number (HOB=1)

Cylinder Low (HOB=0)

Cylinder Low (HOB=1)

Cylinder High (HOB=0)

Cylinder High (HOB=1)

Table 95   Abort Type Field

Abort Type Parameters		
Abort Type	Abort Type	Description
0h	Abort All	The device attempts to abort all outstanding NCQ commands.
1h	Abort Streaming	The device attempts to abort all outstanding NCQ Streaming commands. All non-streaming NCQ commands are unaffected.
2h	Abort Non-Streaming	The device attempts to abort all outstanding NCQ Non-Streaming commands. All NCQ Streaming commands are unaffected.
3h	Abort Selected	The device attempts to abort the outstanding NCQ command associated with the tag represented in TTAG field.

11.11.2 Deadline handling Subcommand (1h)

Table 96   Deadline handling Subcommand (1h)

Command Block Output Registers		7	6	5	4	3	2	1	0
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Feature	Current	-	-	V	V	0	0	0	1
	Previous	-	-	-	-	-	-	-	-
Sector Count	Current	V	V	V	V	V	-	-	-
	Previous	-	-	-	-	-	-	-	-
Sector Number	Current	V	V	V	V	V	-	-	-
	Previous	-	-	-	-	-	-	-	-
Cylinder Low	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Cylinder High	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Device/Head		-	1	-	0	-	-	-	-
Command		0	1	1	0	0	0	1	1

Command Block Input Registers		7	6	5	4	3	2	1	0
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Error		...See Below...							
Sector Count	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Sector Number	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Cylinder Low	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Cylinder High	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Device/Head		-	-	-	-	-	-	-	-
Status		…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
V	V	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Normal Outputs

If this Deadline Handling Subcommand command is supported, the device returns the command completed with no error.

When a Deadline Handling Subcommand command completes successfully, a Set Device Bits FIS is sent to the host to complete the Deadline Handling subcommand. This SDB FIS may also indicate other completed commands.

Error Outputs

The device returns command aborted if:

a) NCQ is disabled and a DEADLINE HANDLING command is issued to the device;

b) The value of the TTAG field equals the value of the TAG field;

c) The value of the TTAG field is an invalid TAG number; or

d) An unsupported Abort type parameter is specified.

Output Parameters To The Device
Feature Current

> **Subcommand (bits 3-0)**   When bits (3:0) is 1h, Deadline Handling Subcommand.

> **WDNC(bits 4)**   If the WDNC (Write Data Not Continue) bit is cleared to zero, then the device allows WRITE FPDMA QUEUED command completion times to exceed what the ICC parameter specified. If the WDNC bit is set to one, then the all WRITE FPDMA QUEUED commands are completed by the time specified by the ICC timer value, otherwise the device returns command aborted for all outstanding commands. WDNC is only applicable to WRITE FPDMA QUEUED commands with PRIO is set to 01b (Isochronous – deadline dependent priority)

> **RDNC(bits 5)**   If the RDNC (Read Data Not Continue) bit is cleared to zero, then the device allows READ FPDMA QUEUED command completion times to exceed what the ICC parameter specified. If the RDNC bit is set to one, then the all READ FPDMA QUEUED commands are completed by the time specified by the ICC timer value, otherwise the device returns command aborted for all outstanding commands. RDNC is only applicable to READ FPDMA QUEUED commands with PRIO is set to 01b (Isochronous – deadline dependent priority)

Feature Previous
Sector Count Current

> **TAG (bits 7-3)**   The TAG value is assigned to be different from all other queued commands. The value does not exceed the maximum queue depth specified by the Word 75 of the Identify Device information.

Sector Count Previous
Sector Number Current
Cylinder Low Current
Cylinder Low Previous
Cylinder High Current
Cylinder High Previous
Device/Head

Input Parameters From The Device
Sector Number (HOB=0)
Sector Number (HOB=1)
Cylinder Low (HOB=0)
Cylinder Low (HOB=1)
Cylinder High (HOB=0)
Cylinder High (HOB=1)

11.11.3 Set Features Subcommand (5h)

Table 97 SET FEATURES Subcommand (5h)

Command Block Output Registers		7	6	5	4	3	2	1	0
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Feature	Current	-	-	V	V	0	1	0	1
	Previous	-	-	-	-	-	-	-	-
Sector Count	Current	V	V	V	V	V	-	-	-
	Previous	-	-	-	-	-	-	-	-
Sector Number	Current	V	V	V	V	V	-	-	-
	Previous	-	-	-	-	-	-	-	-
Cylinder Low	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Cylinder High	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Device/Head		-	1	-	0	-	-	-	-
Command		0	1	1	0	0	0	1	1

Command Blck Input Registers		7	6	5	4	3	2	1	0
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Error					...See Below...				
Sector Count	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Sector Number	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Cylinder Low	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Cylinder High	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Device/Head		-	-	-	-	-	-	-	-
Status					…See Below…				

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
V	V	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Normal Outputs
Upon successful completion of one or more outstanding commands, the device shall transmit a Set Device Bits FIS with the Interrupt bit set to one and one or more bits set to one in the ACT field corresponding to the bit position for each command TAG that has completed since the last status notification was transmitted. The ERR bit in the Status register shall be cleared to zero and the value in the Error register shall be zero.

Error Outputs
If the device has received a command that has not yet been acknowledged by clearing the BSY bit to zero and an error is encountered, the device shall transmit a Register Device to Host FIS (see Table 127) with the ERR bit set to one and the BSY bit cleared to zero in the Status field, the ATA error code in the Error field.

Output Parameters To The Device

Feature Current

Subcommand (bits 3-0)	When bits(3:0) is 5h, SET FEATURES Subcommand.
Subcommand Specific (bits 7-4)	

Feature Previous   Contents of SET FEATURES (15:8) field

Sector Count Current

TAG (bits 7-3)	The TAG value is assigned to be different from all other queued commands. The value does not exceed the maximum queue depth specified by the Word 75 of the Identify Device information.

Sector Count Previous   Contents of SET FEATURES LBA(7:0) field LBA (7:0).

Sector Number Current   Contents of SET FEATURES LBA(27:24)

Cylinder Low Current   Contents of SET FEATURES LBA(15:8)

Cylinder Low Previous

Cylinder High Current   Contents of SET FEATURES LBA(23:16)

Cylinder High Previous

Device/Head

Input Parameters From The Device

Sector Number (HOB=0)

Sector Number (HOB=1)

Cylinder Low (HOB=0)

Cylinder Low (HOB=1)

Cylinder High (HOB=0)

Cylinder High (HOB=1)

11.12 RECEIVE FPDMA QUEUED (65h)

Table 98 RECEIVE FPDMA QUEUED command (65h)

Command Block Output Registers		7	6	5	4	3	2	1	0
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Feature	Current	V	V	V	V	V	V	V	V
	Previous	-	-	-	-	-	-	-	-
Sector Count	Current	V	V	V	V	V	-	-	-
	Previous	V	V	-	-	-	-	-	-
Sector Number	Current	V	V	V	V	V	-	-	-
	Previous	-	-	-	-	-	-	-	-
Cylinder Low	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Cylinder High	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Device/Head		-	1	-	0	-	-	-	-
Command		0	1	1	0	0	1	0	1

Command Block Input Registers		7	6	5	4	3	2	1	0
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Error		...See Below...							
Sector Count	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Sector Number	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Cylinder Low	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Cylinder High	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Device/Head		-	-	-	-	-	-	-	-
Status		…See Below…							

Error Register

7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
V	V	0	V	0	V	0	0

Status Register

7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	0	-	-	V

Table 99 defines the RECEIVE FPDMA QUEUED subcommands. See the referenced sections for additional information in this table.

Table 99 RECEIVE FPDMA QUEUED Subcommand Field

Subcommand	Description	Reference
0h	Reserved	-
1h	READ LOG DMA EXT	11.16.1 READ LOG DMA EXT (1h)
2h - Fh	Reserved	-

The output from the host to the device, the command acceptance outputs for this command, the normal outputs for this command and the error outputs for this command are subcommand specific. See 11.16.1 READ LOG DMA EXT (1h).

11.12.1　READ LOG DMA EXT (1h)

Table 100　READ LOG DMA EXT Subcommand (1h)

Command Block Output Registers		7	6	5	4	3	2	1	0
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Feature	Current	V	V	V	V	0	0	0	1
	Previous	-	-	-	-	-	-	-	-
Sector Count	Current	V	V	V	V	V	-	-	-
	Previous	-	-	-	-	-	-	-	-
Sector Number	Current	V	V	V	V	V	-	-	-
	Previous	-	-	-	-	-	-	-	-
Cylinder Low	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Cylinder High	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Device/Head		-	1	-	0	-	-	-	-
Command		0	1	1	0	0	0	1	1

Command Block Input Registers		7	6	5	4	3	2	1	0
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Error				...See Below...					
Sector Count	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Sector Number	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Cylinder Low	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Cylinder High	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Device/Head		-	-	-	-	-	-	-	-
Status				…See Below…					

Error Register

7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
V	V	0	V	0	V	0	0

Status Register

7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	0	-	-	V

Normal Outputs

Upon successful completion of one or more outstanding commands, the device shall transmit a Set Device Bits FIS with the Interrupt bit set to one and one or more bits set to one in the ACT field corresponding to the bit position for each command TAG that has completed since the last status notification was transmitted.

Error Outputs

If the device has received a command that has not yet been acknowledged by clearing the BSY bit to zero and an error is encountered, the device shall transmit a Register Device to Host FIS.

Output Parameters To The Device

Feature Current	Contents of READ LOG DMA EXT Count(7:0) field
Subcommand (bits 4-0)	When bits (4:0) is 01h, Read Log DMA Ext Subcommand.
Subcommand Specific (bits 7-4)	
Feature Previous	Contents of READ LOG DMA EXT Count(15:8) field
Sector Count Current	
TAG (bits 7-3)	
Sector Count Previous	
Sector Number Current	Contents of READ LOG DMA EXT LBA(7:0) field
Sector Number Previous	Contents of READ LOG DMA EXT LBA(31:24) field
Cylinder Low Current	Contents of READ LOG DMA EXT LBA(15:8) field
Cylinder Low Previous	Contents of READ LOG DMA EXT LBA(39:32) field
Cylinder High Current	Contents of READ LOG DMA EXT LBA(23:16) field

Cylinder High Previous   Contents of READ LOG DMA EXT LBA(47:40) field

Device/Head

Input Parameters From The Device

Sector Number (HOB=0)

Sector Number (HOB=1)

Cylinder Low (HOB=0)

Cylinder Low (HOB=1)

Cylinder High (HOB=0)

Cylinder High (HOB=1)

11.13   SEND FPDMA QUEUED (64h)

Table 101   SEND FPDMA QUEUED command (64h)

Command Block Output Registers		7	6	5	4	3	2	1	0
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Feature	Current	V	V	V	V	V	V	V	V
	Previous	-	-	-	-	-	-	-	-
Sector Count	Current	V	V	V	V	V	-	-	-
	Previous	V	V	-	-	-	-	-	-
Sector Number	Current	V	V	V	V	V	-	-	-
	Previous	-	-	-	-	-	-	-	-
Cylinder Low	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Cylinder High	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Device/Head		-	1	-	0	-	-	-	-
Command		0	1	1	0	0	1	0	0

Command Block Input Registers		7	6	5	4	3	2	1	0
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Error				...See Below...				
Sector Count	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Sector Number	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Cylinder Low	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Cylinder High	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Device/Head		-	-	-	-	-	-	-	-
Status				…See Below…				

Error Register

7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
V	V	0	V	0	V	0	0

Status Register

7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	0	-	-	V

Table 102 defines the SEND FPDMA QUEUED subcommands. See the referenced sections for additional information in this table.

Table 102   SEND FPDMA QUEUED Subcommand Field

Subcommand	Description	Reference
0h – 1h	Reserved	-
2h	WRITE LOG DMA EXT	11.17.1 WRITE LOG DMA EXT (2h)
3h – Fh	Reserved	-

The output from the host to the device, the command acceptance outputs for this command, the normal outputs for this command and the error outputs for this command are subcommand specific.

11.13.1   WRITE LOG DMA EXT (2h)

Table 103   WRITE LOG DMA EXT Subcommand (2h)

Command Block Output Registers		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Feature	Current	V	V	V	V	0	0	1	0
	Previous	-	-	-	-	-	-	-	-
Sector Count	Current	V	V	V	V	V	-	-	-
	Previous	-	-	-	-	-	-	-	-
Sector Number	Current	V	V	V	V	V	-	-	-
	Previous	-	-	-	-	-	-	-	-
Cylinder Low	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Cylinder High	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Device/Head		-	1	-	0	-	-	-	-
Command		0	1	1	0	0	1	0	0

Command Block Input Registers		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Error				...See Below...					
Sector Count	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Sector Number	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Cylinder Low	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Cylinder High	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Device/Head		-	-	-	-	-	-	-	-
Status				…See Below…					

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
V	V	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	0	-	-	V

Normal Outputs

Upon successful completion of one or more outstanding commands, the device shall transmit a Set Device Bits FIS with one or more bits set to one in the ACT field corresponding to the bit position for each command TAG that has completed since the last status notification was transmitted.

Error Outputs

If the device has received a command that has not yet been acknowledged by clearing the BSY bit to zero and an error is encountered, the device shall transmit a Register Device to Host FIS.

Output Parameters To The Device

Feature Current	Contents of WRITE LOG DMA EXT Count(7:0) field
Subcommand (bits 4-0)	When bits (4:0) is 02h, Read Log DMA Ext Subcommand.
Subcommand Specific (bits 7-4)	
Feature Previous	Contents of WRITE LOG DMA EXT Count(15:8) field
Sector Count Current	
TAG (bits 7-3)	
Sector Count Previous	
Sector Number Current	Contents of WRITE LOG DMA EXT LBA(7:0) field
Sector Number Previous	Contents of WRITE LOG DMA EXT LBA(31:24) field
Cylinder Low Current	Contents of WRITE LOG DMA EXT LBA(15:8) field
Cylinder Low Previous	Contents of WRITE LOG DMA EXT LBA(39:32) field

Cylinder High Current   Contents of WRITE LOG DMA EXT LBA(23:16) field
Cylinder High Previous Contents of WRITE LOG DMA EXT LBA(47:40) field
Device/Head

Input Parameters From The Device
Sector Number (HOB=0)
Sector Number (HOB=1)
Cylinder Low (HOB=0)
Cylinder Low (HOB=1)
Cylinder High (HOB=0)
Cylinder High (HOB=1)

11.14   Read Buffer (E4h)

The Read Buffer command transfers a sector of data from the sector buffer of device to the host.

The sector is transferred through the Data Register 16 bits at a time.

The sector transferred will be from the same part of the buffer written to by the last Write Buffer command. The contents of the sector may be different if any reads or writes have occurred since the Write Buffer command was issued.

Table 104   Read Buffer Command (E4h)

Command Block Output Registers	7	6	5	4	3	2	1	0	Command Block Input Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0	Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-	Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-	Error				...See Below...				
Sector Count	-	-	-	-	-	-	-	-	Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-	Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-	Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-	Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-	Device/Head	-	-	-	-	-	-	-	-
Command	1	1	1	0	0	1	0	0	Status				...See Below...				

Error Register									Status Register								
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	0	0	V	0	0		0	V	0	-	-	0	-	V

11.15   Read Buffer DMA (E9h)

The Read Buffer DMA command transfers a sector of data from the sector buffer of device to the host.

The sector is transferred through the Data Register 16 bits at a time.

The sector transferred will be from the same part of the buffer written to by the last Write Buffer command. The contents of the sector may be different if any reads or writes have occurred since the Write Buffer command was issued.

Table 105   Read Buffer DMA Command (E9h)

Command Block Output Registers										Command Block Input Registers									
Register	7	6	5	4	3	2	1	0		Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-		Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-		Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-		Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-		Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-		Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-		Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-		Device/Head	-	-	-	-	-	-	-	-
Command	1	1	1	0	1	0	0	1		Status	...See Below...							

Error Register								Status Register							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN	BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	0	0	V	0	0	0	V	0	-	-	0	-	V

11.16   Read DMA (C8h/C9h)

The Read DMA command reads one or more sectors of data from disk media, then transfers the data from the device to the host.

The sectors are transferred through the Data Register 16 bits at a time.

The host initializes a slave-DMA channel prior to issuing the command. The data transfers are qualified by DMARQ and are performed by the slave-DMA channel. The device issues only one interrupt per command to indicate that data transfer has terminated and status is available.

If an uncorrectable error occurs, the read will be terminated at the failing sector.

Table 106   Read DMA Command (C8h/C9h)

Command Block Output Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	1	L	1	D	H	H	H	H
Command	1	1	0	0	1	0	0	R

Command Block Input Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	-	-	-	-	H	H	H	H
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
V	V	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Output Parameters To The Device

Sector Count   The number of continuous sectors to be transferred. If zero is specified, then 256 sectors will be transferred.

Sector Number   The sector number of the first sector to be transferred. (L=0)
In LBA mode, this register specifies LBA address bits 0-7 to be transferred. (L=1)

Cylinder High/Low   The cylinder number of the first sector to be transferred. (L=0)
In LBA mode, this register specifies LBA address bits 8-15 (Low) 16-23 (High) to be transferred. (L=1)

H   The head number of the first sector to be transferred. (L=0)
In LBA mode, this register specifies LBA bits 24-27 to be transferred. (L=1)

R   The retry bit, but this bit is ignored.

Input Parameters From The Device

Sector Count   The number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs.

Sector Number   The sector number of the last transferred sector. (L=0)
In LBA mode, this register contains current LBA bits 0-7. (L=1)

Cylinder High/Low   The cylinder number of the last transferred sector. (L=0)
In LBA mode, this register contains current LBA bits 8-15 (Low), 16-23 (High). (L=1)

H   The head number of the sector to be transferred. (L=0)
In LBA mode, this register contains current LBA bits 24-27. (L=1)

11.17   Read DMA Ext (25h)

The Read DMA command reads one or more sectors of data from disk media, and then transfers the data from the device to the host.

The sectors are transferred through the Data Register 16 bits at a time.

The host initializes a slave-DMA channel prior to issuing the command. The data transfers are qualified by DMARQ and are performed by the slave-DMA channel. The device issues only one interrupt per command to indicate that data transfer has terminated and status is available.

If an uncorrectable error occurs, the read will be terminated at the failing sector.

Table 107   Read DMA Ext Command (25h)

Command Block Output Registers		7	6	5	4	3	2	1	0
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Feature	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Sector Count	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Sector Number	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder Low	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder High	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Device/Head		1	1	1	D	-	-	-	-
Command		0	0	1	0	0	1	0	1

Command Block Input Registers		7	6	5	4	3	2	1	0
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Error					...See Below...				
Sector Count	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Sector Number	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Cylinder Low	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Cylinder High	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Device/Head		-	-	-	-	-	-	-	-
Status					...See Below...				

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
V	Vs	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Output Parameters To The Device

Sector Count Current   The number of sectors to be transferred low order, bits (7:0).

Sector Count Previous   The number of sectors to be transferred high order, bits (15:8).   If 0000h in the Sector Count register is specified, then 65,536 sectors will be transferred.

Sector Number Current   LBA (7:0)

Sector Number Previous   LBA (31:24)

Cylinder Low Current   LBA (15:8)

Cylinder Low Previous   LBA (39:32)

Cylinder High Current   LBA (23:16)

Cylinder High Previous   LBA (47:40)

Input Parameters From The Device

Sector Number (HOB=0)   LBA (7:0) of the address of the first unrecoverable error.

Sector Number (HOB=1)   LBA (31:24) of the address of the first unrecoverable error.

Cylinder Low (HOB=0)   LBA (15:8) of the address of the first unrecoverable error.

Cylinder Low (HOB=1)   LBA (39:32) of the address of the first unrecoverable error.

Cylinder High (HOB=0)   LBA (23:16) of the address of the first unrecoverable error.

Cylinder High (HOB=1)   LBA (47:40) of the address of the first unrecoverable error.

11.18 Read FPDMA Queued (60h)

The Read FPDMA command reads one or more sectors of data from disk media, and then transfers the data from the device to the host.

If an uncorrectable error occurs, the read will be terminated at the failing sector.

Table 108 Read FPDMA Queued Command (60h)

Command Block Output Registers		7	6	5	4	3	2	1	0
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Feature	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Sector Count	Current	V	V	V	V	V	-	-	-
	Previous	-	-	-	-	-	-	-	-
Sector Number	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder Low	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder High	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Device/Head		V	1	0	0	-	-	-	-
Command		0	1	1	0	0	0	0	0

Command Block Input Registers		7	6	5	4	3	2	1	0
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Error					...See Below...				
Sector Count	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Sector Number	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Cylinder Low	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Cylinder High	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Device/Head		-	-	-	-	-	-	-	-
Status					…See Below…				

Error Register								
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
V	Vs	0	V	0	V	0	0

Status Register								
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Output Parameters To The Device

Feature Current   The number of sectors to be transferred low order, bits (7:0).

Feature Previous   The number of sectors to be transferred high order, bits (15:8).

Sector Count Current

   TAG (bits 7-3)   The TAG value shall be assigned to be different from all other queued commands. The value shall not exceed the maximum queue depth specified by the Word 75 of the Identify Device information.

   RARC (bits 0)   If the Rebuild Assist feature is not supported, then the RARC bit shall be ignored.

                  If the Rebuild Assist feature is supported and is disabled, then the RARC bit shall be ignored.

                  If the Rebuild Assist feature is supported and enabled, then the RARC bit specifies that read operations shall be processed as defined in 9.17.5 Rebuild Assist log (15h).

Sector Count Previous

   PRIO (bits 7-6)   The Priority (PRIO) value shall be assigned by the host based on the priority of the command issued. The device makes a best effort to complete High priority requests in a more timely fashion than Normal and isochronous priority requests. The device tries to complete isochronous requests prior to its associated deadline. The Priority values are defined as follows:

               00b   Normal priority

               01b   Isochronous – deadline dependent priority

               10b   High priority

Sector Number Current	LBA (7:0)
Sector Number Previous	LBA (31:24)
Cylinder Low Current	LBA (15:8)
Cylinder Low Previous	LBA (39:32)
Cylinder High Current	LBA (23:16)
Cylinder High Previous	LBA (47:40)

ZCICC   The Isochronous Command Completion (ICC) field is valid when PRIO is set to a value of 01b. It is assigned by the host based on the intended deadline associated with the command issued. When a deadline has expired, the device continues to complete the command as soon as possible. The host can modify this behavior if the device supports the NCQ NON-DATA command (see 11.15 NCQ NON-DATA (63h)) and supports the Deadline Handling subcommand (see 11.15.2 Deadline handling Subcommand (1h)). This subcommand allows the host to set whether the device aborts commands that have exceeded the time set in ICC.

There are several parameters encoded in the ICC field: Fine or Coarse timing, Interval and the Max Time. The Interval indicates the time units of the Time Limit parameter.

If ICC Bit 7 cleared to zero, then the time interval is fine-grained.

    Interval   = 10msec

    Time Limit   = (ICC[6:0] + 1) * 10 msec

If ICC Bit 7 is set to one (coarse encoding), then the time interval is coarse grained.

    Interval   = 0.5 sec

    Time Limit   = (ICC[6:0] + 1) * 0.5 sec

Device/Head

   FUA (bit 7)   When the FUA bit is set to 1, the requested data is always retrieved from the media regardless of whether the data are held in the sector buffer or not.

When the FUA bit is set to 0, the data may be retrieved from the media or from the cached data left by previously processed Read or Write commands.

Input Parameters From The Device

Sector Number (HOB=0)	LBA (7:0) of the address of the first unrecoverable error.
Sector Number (HOB=1)	LBA (31:24) of the address of the first unrecoverable error.
Cylinder Low (HOB=0)	LBA (15:8) of the address of the first unrecoverable error.
Cylinder Low (HOB=1)	LBA (39:32) of the address of the first unrecoverable error.
Cylinder High (HOB=0)	LBA (23:16) of the address of the first unrecoverable error.
Cylinder High (HOB=1)	LBA (47:40) of the address of the first unrecoverable error.

11.19 Read Log Ext (2Fh)

This command returns the specified log to the host. The device shall interrupt for each DRQ block transferred.

Table 109 Read Log Ext Command (2Fh

Command Block Output Registers		7	6	5	4	3	2	1	0
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Feature	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Sector Count	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Sector Number	Current	V	V	V	V	V	V	V	V
	Previous	-	-	-	-	-	-	-	-
Cylinder Low	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder High	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Device/Head		1	-	1	D	-	-	-	-
Command		0	0	1	0	1	1	1	1

Command Block Input Registers		7	6	5	4	3	2	1	0
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Error		...See Below...							
Sector Count	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Sector Number	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Cylinder Low	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Cylinder High	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Device/Head		-	-	-	-	-	-	-	-
Status		...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	V	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Output Parameters To The Device

Feature	Log Address Specific
Sector Count Current	The number of sectors to be read from the specified log low order, bits (7:0). The log transferred by the drive shall start at the sector in the specified log at the specified offset, regardless of the sector count requested.
Sector Count Previous	The number of sectors to be read from the specified log high orders, bits (15:8).
Sector Number Current	The log to be returned as described in Table 140.
Cylinder Low Current	The first sector of the log to be read low order, bits (7:0).
Cylinder Low Previous	The first sector of the log to be read high order, bits (15:8).

Table 110   Log Address Definition

Log address	Content	Feature set	Type
00h	Log directory	N/A	Read Only
03h	Extended Comprehensive SMART error log	SMART error logging	Read Only
04h	Device Statistics	N/A	Read Only
06h	SMART self-test log	SMART self-test	See Note
07h	Extended SMART self-test log	SMART self-test	Read Only
08h	Power Conditions log	Extended Power Condition	Read Only
10h	Command Error	Native Command Queuing	Read Only
11h	Phy Event Counters	Serial ATA	Read Only
12h	NCQ NON-DATA log	NCQ NON-DATA	Read Only
2Fh	Sector Configuration log	N/A	Read Only
30h	Identify Device Data log	N/A	Read Only
80h-9Fh	Host vendor specific	SMART	Read/Write

Note: If log address 06h is accessed using the Read Log Ext or Write Log Ext commands, command abort shall be returned.

Note: Please see *Section 9.18* about Phy Event Counters.

Note: Please see *Section 9.18.4* about NCQ NON-DATA (63h).

Table 111   Log Address Definition for Serial ATA

Log Address	Description
00h - 0Fh	As defined in the ACS-2 standard
10h	NCQ Queued Error log
11h	Phy Event Counters log
12h	NCQ NON-DATA log
13h	Reserved
14h	Reserved
15h	Rebuild Assist log
16h - 17h	Reserved
18h - FFh	As defined in the ACS-2 standard

The Extended SMART self-test log sector shall support 48-bit and 28-bit addressing. All 28-bit entries contained in the SMART self-test log sector shall also be included in the Comprehensive SMART self-test log sector with the 48-bit entries.

If the feature set associated with the log specified in the Sector Number register is not supported or enabled, or if the values in the Sector Count, Sector Number or Cylinder Low registers are invalid, the device shall return command aborted.

11.19.1　General Purpose Log Directory

Table 112 defines the 512 bytes that make up the General Purpose Log Directory.

Table 112   General Purpose Log Directory

Description	Bytes	Offset
General Purpose Logging Version	2	00h
Number of sectors in the log at log address 01h (7:0)	1	02h
Number of sectors in the log at log address 01h (15:8)	1	03h
Number of sectors in the log at log address 02h (7:0)	1	04h
Number of sectors in the log at log address 02h (15:8)	1	05h
...		
Number of sectors in the log at log address 20h (7:0)	1	40h
Number of sectors in the log at log address 20h (15:8)	1	41h
...		
Number of sectors in the log at log address 80h (7:0)	1	100h
Number of sectors in the log at log address 80h (15:8)	1	101h
...		
Number of sectors in the log at log address FFh (7:0)	1	1FEh
Number of sectors in the log at log address FFh (15:8)	1	1FFh
	512	

The value of the General Purpose Logging Version word shall be 0001h. A value of 0000h indicates that there is no General Purpose Log Directory.

The logs at log addresses 80-9Fh shall each be defined as 16 sectors long.

Table 113 defines the 512 bytes that make up the General Purpose Log Directory for Serial ATA.

Table 113   General Purpose Log Directory for Serial ATA

Byte	Log	Value
000h..01Fh		As defined in the ACS-2 standard
020h	10h	1 if Native Command Queuing is supported, 0 if Native Command Queuing is not supported
021h	10h	0
022h	11	1 if Phy Event Counters are supported 0 if Phy Event Counters are not supported
023h	11h	0
024h	12h	1 if NCQ NON-DATA is supported 0 if NCQ NON-DATA is not supported
025h	12h	0
026h		Reserved
027h		Reserved
028h		Reserved
029h		Reserved
02Ah	15h	1 if Rebuild Assist log is supported 0 if Rebuild Assist log is not supported
02Bh	15h	0
02Ch..2Fh		Reserved
030h..1FFh		As defined in the ACS-2 standard

11.19.2 Extended Comprehensive SMART Error Log

Table 114 defines the format of each of the sectors that comprise the Extended Comprehensive SMART error log. Error log data structure shall not include errors attributed to the receipt of faulty commands such as command codes not implemented by the device or requests with invalid parameters or in valid addresses.

Table 114   Extended Comprehensive SMART Error Log

Description	Bytes	Offset
SMART error log version	1	00h
Reserved	1	01h
Error log index (7:0)	1	02h
Error log index (15:8)	1	03h
1st error log data structure	124	04h
2nd error log data structure	124	80h
3rd error log data structure	124	FCh
4th error log data structure	124	178h
Device error count	2	1F4h
Reserved	9	1F6h
Data structure checksum	1	1FFh
	512	

11.19.2.1 Error Log Version

The value of this version shall be 01h.

11.19.2.2 Error Log Index

This indicates the error log data structure representing the most recent error. If there have been no error log entries, it is cleared to 0. Valid values for the error log index are 0 to 4.

11.19.2.3 Extended Error Log Data Structure

An error log data structure shall be presented for each of the last four errors reported by the device.
These error log data structure entries are viewed as a circular buffer. The fifth error shall create an error log structure that replaces the first error log data structure. The next error after that shall create an error log data structure that replaces the second error log structure, etc.
Unused error log data structures shall be filled with zeros.

Data format of each error log structure is shown below.

Table 115   Extended Error Log Data Structure

Description	Bytes	Offset
1st command data structure	18	00h
2nd command data structure	18	12h
3rd command data structure	18	24h
4th command data structure	18	36h
5th command data structure	18	48h
Error data structure	34	5Ah
	124	

Command data structure: Data format of each command data structure is shown below.

Table 116   Command Data Structure

Description	Bytes	Offset
Device Control register	1	00h
Features register (7:0) (see Note)	1	01h
Features register (15:8)	1	02h
Sector count register (7:0)	1	03h
Sector count register (15:8)	1	04h
Sector number register (7:0)	1	05h
Sector number register (15:8)	1	06h
Cylinder Low register (7:0)	1	07h
Cylinder Low register (15:8)	1	08h
Cylinder High register (7:0)	1	09h
Cylinder High register (15:8)	1	0Ah
Device/Head register	1	0Bh
Command register	1	0Ch
Reserved	1	0Dh
Timestamp (milliseconds from Power-on)	4	0Eh
	18	

Note: bits (7:0) refer to the most recently written contents of the register. Bits (15:8) refer to the contents of the register prior to the most recent write to the register.

Error data structure: Data format of error data structure is shown below.

Table 117   Error Data Structure

Description	Bytes	Offset
Reserved	1	00h
Error register	1	01h
Sector count register (7:0) (see Note)	1	02h
Sector count register (15:8) (see Note)	1	03h
Sector number register (7:0)	1	04h
Sector number register (15:8)	1	05h
Cylinder Low register (7:0)	1	06h
Cylinder Low register (15:8)	1	07h
Cylinder High register (7:0)	1	08h
Cylinder High register (15:8)	1	09h
Device/Head register	1	0Ah
Status register	1	0Bh
Extended error data (vendor specific)	19	0Ch
State	1	1Fh
Life timestamp (hours)	2	20h
	34	

Note: bits (7:0) refer to the contents if the register is read with bit 7 of the Device Control register cleared to zero. Bits (15:8) refer to the contents if the register is read with bit 7 of the Device Control register set to one.

State shall contain a value indicating the state of the device when the command was issued to the device or the reset occurred as described below.

Value	State
x0h	Unknown
x1h	Sleep
x2h	Standby (If the EPC feature set is enabled, Standby is standby_y or standby_z)
x3h	Active/Idle
	(If the EPC feature set is enabled, Active/Idle is idle_a or idle_b or idle_c)
x4h	SMART Off-line or Self-test
x5h-xAh	Reserved
xBh-xFh	Vendor specific

Note: The value of x is vendor specific.

11.19.2.4   Device Error Count

This field shall contain the total number of errors attributable to the device that have been reported by the device during the life of the device. This count shall not include errors attributed to the receipt of faulty commands such as commands codes not implemented by the device or requests with invalid parameters or invalid addresses. If the maximum value for this field is reached the count shall remain at the maximum value when additional errors are encountered and logged.

11.19.3　Device Statistics Log

The Device Statistics log contains selected statistics about the device.

The number of log pages may be greater than one.

See Table 118 for a list of defined log pages. Each supported log page consists of a header field that may be followed by defined statistics fields. If the Revision Number field in the log page header is 0000h, then that log page is not supported. All log page data following the last defined statistic for that log page is reserved.

If an unsupported log page is requested, then 512 bytes of all zeros are returned for that log page.

Table 118　Defined Device Statistics Log Pages

Description	Log page
List of supported log pages (*Table 118*)	00h
General Statistics (*Table 120*)	01h
Rotating Media Statistics (*Table 121*)	03h
General Errors Statistics (*Table 122*)	04h
Temperature Statistics (*Tables 123-124*)	05h
Transport Statistics (*Table 125*)	06h
Reserved	08h..Ffh

11.19.3.1　List of Supported Device Statistics Log Pages (log page 00h)

The List of Supported Device Statistics log pages contains a list of the supported device statistics log pages. Entries are in order of ascending log page number. Every log page for which there is at least one supported statistic is listed.

Table 119　List of supported Device Statistics Log Pages

Description	Bytes	Offset
Device Statistics Information Header. This device statistics log page lists the number of the supported device statistics log pages. Bit Description 63:24 Reserved 23:16 Log page number. (00h) 15:0 Revision number. (0001h)	8	00h
Number of entries (n) in the following list	1	08h
Log page number of first supported device statistics log page (00h)	1	09h
Log page number of second supported device statistics log page	1	0Ah
…		
Log page number of nth supported device statistics log page	1	n+08h
Reserved		n+09h..1FFh

11.19.3.2   General Statistics (log page 01h)

The General Statistics log page contains general information about the device.

Table 120   General Statistics

Description		Bytes	Offset
Device Statistics Information Header		8	00h
Bit	Description		
63:24	Reserved		
23:16	Log page number. (01h)		
15:0	Revision number. (0002h)		
Lifetime Power-On Resets		8	08h
Bit	Description		
63:56	Device Statistics Flags		
55:32	Reserved		
31:0	Number of times that the device has processed a Power-On Reset event (DWord)		
Power-on Hours		8	10h
Bit	Description		
63:32	Reserved		
31:0	Power-on Hours (DWord)		
Logical Sectors Written		8	18h
Bit	Description		
63:56	Device Statistics Flags		
55:48	Reserved		
47:0	Logical Sectors Written		
Number of Write Commands		8	20h
Bit	Description		
63:56	Device Statistics Flags		
55:48	Reserved		
47:0	Number of Write Commands		
Logical Sectors Read		8	28h
Bit	Description		
63:56	Device Statistics Flags		
55:48	Reserved		
47:0	Logical Sectors Read		
Number of Read Commands		8	30h
Bit	Description		
63:56	Device Statistics Flags		
55:48	Reserved		
47:0	Number of Read Commands		
Reserved		1	38h..1Ffh

11.19.3.3   Rotating Media Statistics (log page 03h)

The Rotating Media Statics log page contains device rotating media information.

Table 121   Rotating Media Statistics

Description		Bytes	Offset
Device Statistics Information Header		8	00h
Bit	Description		
63:24	Reserved		
23:16	Log page number. (03h)		
15:0	Revision number. (0001h)		
Spindle Motor Power-on Hours		8	08h
Bit	Description		
63:56	Device Statistics Flags		
55:32	Reserved		
31:0	Spindle Motor Power-on Hours (DWord)		
Head Flying Hours		8	10h
Bit	Description		
63:56	Device Statistics Flags		
55:32	Reserved		
31:0	Head Flying Hours (DWord)		
Head Load Events		8	18h
Bit	Description		
63:56	Device Statistics Flags		
55:32	Reserved		
31:0	Head Load Events (DWord)		
Number of Reallocated Logical Sectors		8	20h
Bit	Description		
63:56	Device Statistics Flags		
55:32	Reserved		
31:0	Number of Reallocated Logical Sectors (DWord)		
Read Recovery Attempts		8	28h
Bit	Description		
63:56	Device Statistics Flags		
55:32	Reserved		
31:0	Read Recovery Attempts (DWord)		
Number of Mechanical Start Failures		8	30h
Bit	Description		
63:56	Device Statistics Flags		
55:32	Reserved		
31:0	Number of Mechanical Start Failures (DWord)		
Reserved		1	38h..1Ffh

11.19.3.4 General Errors Statistics (log page 04h)

General Errors Statistics log page contains general error information about the device.

Table 122 General Error Statistics

Description		Bytes	Offset
Device Statistics Information Header		8	00h
Bit	Description		
63:24	Reserved		
23:16	Log page number. (04h)		
15:0	Revision number. (0001h)		
Number of Reported Uncorrectable Errors		8	08h
Bit	Description		
63:56	Device Statistics Flags		
55:32	Reserved		
31:0	Number of Reported Uncorrectable Errors (DWord)		
Number of Resets Between Command Acceptance and Command Completion		8	10h
Bit	Description		
63:56	Device Statistics Flags		
55:32	Reserved		
31:0	Number of Resets Between Command Acceptance and Command Completion (DWord)		
Reserved		1	18h..1Ffh

11.19.3.5 Temperature Statistics (log page 05h)

The Temperature Statistics log page contains general information about the device.
The value in the temperature field is a two's complement integer in degrees Celsius.

Table 123 Temperature Statistics (part 1 of 2)

Description		Bytes	Offset
Device Statistics Information Header		8	00h
Bit	Description		
63:24	Reserved		
23:16	Log page number. (05h)		
15:0	Revision number. (0001h)		
Current Temperature		8	08h
Bit	Description		
63:56	Device Statistics Flags		
55:8	Reserved		
7:0	Current Temperature (signed byte)		
Average Short Term Temperature		8	10h
Bit	Description		
63:56	Device Statistics Flags		
55:8	Reserved		
7:0	Average Short Term Temperature (signed byte)		
Average Long Term Temperature		8	18h
Bit	Description		
63:56	Device Statistics Flags		
55:8	Reserved		
7:0	Average Long Term Temperature (signed byte)		

Table 124   Temperature Statistics (part 2 of 2)

Highest Temperature			8	20h
Bit	Description			
63:56	Device Statistics Flags			
55:8	Reserved			
7:0	Highest Temperature (signed byte)			
Lowest Temperature			8	28h
Bit	Description			
63:56	Device Statistics Flags			
55:8	Reserved			
7:0	Lowest Temperature (signed byte)			
Highest Average Short Term Temperature			8	30h
Bit	Description			
63:56	Device Statistics Flags			
55:8	Reserved			
7:0	Highest Average Short Term Temperature (signed byte)			
Lowest Average Short Term Temperature			8	38h
Bit	Description			
63:56	Device Statistics Flags			
55:8	Reserved			
7:0	Lowest Average Short Term Temperature (signed byte)			
Highest Average Long Term Temperature			8	40h
Bit	Description			
63:56	Device Statistics Flags			
55:8	Reserved			
7:0	Highest Average Long Term Temperature (signed byte)			
Lowest Average Long Term Temperature			8	48h
Bit	Description			
63:56	Device Statistics Flags			
55:8	Reserved			
7:0	Lowest Average Long Term Temperature (signed byte)			
Time in Over-Temperature			8	50h
Bit	Description			
63:56	Device Statistics Flags			
55:32	Reserved			
31:0	Time in Over-Temperature (DWord)			
Specified Maximum Operating Temperature			8	58h
Bit	Description			
63:56	Device Statistics Flags			
55:8	Reserved			
7:0	Specified Maximum Operating Temperature (signed byte)			

Time in Under-Temperature			8	60h
Bit	Description			
63:56	Device Statistics Flags			
55:32	Reserved			
31:0	Time in Under-Temperature (DWord)			
Specified Minimum Operating Temperature			8	68h
Bit	Description			
63:56	Device Statistics Flags			
55:8	Reserved			
7:0	Specified Minimum Operating Temperature (signed byte)			
Reserved			1	70h..1Ffh

11.19.3.6   Transport Statistics (log page 06h)

The Transport Statistics log page contains interface transport information about the device.

Table 125   Transport Statistics

Description		Bytes	Offset
Device Statistics Information Header		8	00h
Bit	Description		
63:24	Reserved		
23:16	Log page number. (06h)		
15:0	Revision number. (0001h)		
Number of hardware resets		8	08h
Bit	Description		
63:56	Device Statistics Flags		
55:32	Reserved		
31:0	Number of hardware resets (DWord)		
Number of ASR Events		8	10h
Bit	Description		
63:56	Device Statistics Flags		
55:32	Reserved		
31:0	Number of ASR Events (DWord)		
Head Load Events		8	18h
Bit	Description		
63:56	Device Statistics Flags		
55:32	Reserved		
31:0	Head Load Events (DWord)		
Number of Interface CRC Errors		8	20h
Bit	Description		
63:56	Device Statistics Flags		
55:32	Reserved		
31:0	Number of Interface CRC Errors (DWord)		
Reserved		1	28h..1Ffh

11.19.4   Extended Self-Test Log Sector

Table 126 defines the format of each of the sectors that comprise the Extended SMART self-test log.

The Extended SMART self-test log sector shall support 48-bit and 28-bit addressing. All 28-bit entries contained in the SMART self-test log, defined in 11.52.6 Self-Test Log Data Structure on page 288 shall also be included in the Extended SMART self-test log with all 48-bit entries.

Table 126   Extended Self-test Log Data Structure

Description	Bytes	Offset
Self-test log data structure revision number	1	00h
Reserved	1	01h
Self-test descriptor index (7:0)	1	02h
Self-test descriptor index (15:8)	1	03h
Descriptor entry 1	26	04h
Descriptor entry 2	26	1Eh
...		
Descriptor entry 18	26	1D8h
Vendor specific	2	1F2h
Reserved	11	1F4h
Data structure checksum	1	1FFh
	512	

These descriptor entries are viewed as a circular buffer. The nineteenth self-test shall create a descriptor entry that replaces descriptor entry 1. The next self-test after that shall create a descriptor entry that replaces descriptor entry 2, etc. All unused self-test descriptors shall be filled with zeros.

11.19.4.1   Self-Test Log Data Structure Revision Number

The value of this revision number shall be 01h.

11.19.4.2   Self-Test Descriptor Index

This indicates the most recent self-test descriptor. If there have been no self-tests, this is set to zero. Valid values for the Self-test descriptor index are 0 to 18.

11.19.4.3   Extended Self-Test Log Descriptor Entry

The content of the self-test descriptor entry is shown below.

Table 127   Extended Self-test Log Descriptor Entry

Description	Bytes	Offset
Self-test number	1	00h
Self-test execution status	1	01h
Power-on life timestamp in hours	2	02h
Self-test failure check point	1	04h
Failing LBA (7:0)	1	05h
Failing LBA (15:8)	1	06h
Failing LBA (23:16)	1	07h
Failing LBA (31:24)	1	08h
Failing LBA (39:32)	1	09h
Failing LBA (47:40)	1	0Ah
Vendor specific	15	0Bh
	26	

11.19.5   Power Conditions Log

Defines the Power Conditions log. If the Extended Power Conditions feature set is not supported, then the Power Conditions log not is supported. Each Power is composed of the following formats.

Table 128   Idle Power Conditions (Log page 00h)

Offset	Type	Description
0-63	Byte	Idle_a power conditions descriptor. Power condition supported is set to one to indicate that the idle_a power condition is supported.
64-127	Byte	Idle_b power conditions descriptor. Power condition supported is set to one to indicate that the idle_b power condition is supported.
128-191	Byte	Idle_c power conditions descriptor. Power condition supported is set to one to indicate that the idle_c power condition is supported.
192-511	Byte	Reserved

Table 129   Standby Power Conditions (Log page 01h)

Offset	Type	Description
0-383	Byte	Reserved
384-447	Byte	Standby_y power conditions descriptor. Power condition supported is set to one to indicate that the standby_y power condition is supported.
448-511	Byte	Standby_z power conditions descriptor. Power condition supported is set to one to indicate that the standby_z power condition is supported.

Power Conditions log descriptor

Table 130   Power Condition Log Description

Offset	Type	Description
0	Byte	Reserved

1	Byte	Power Condition Flags
		
		Bit Description
		7 Power Condition Supported
		     The Power Condition Supported bit is valid if the EPC feature set is supported, regardless of whether EPC is enabled or disabled. If the Power Condition Supported bit is set to one, then the power condition is supported. If the Power Condition Supported bit is cleared to zero, then the power condition is not supported.
		
		6 Timer Savable
		     The Timer Savable bit is valid if the Power Condition Supported bit is set to one, regardless of whether EPC is enabled or disabled. If the Timer Savable bit is set to one, then the power condition is savable if EPC is enabled. If the Timer Savable bit is cleared to zero, then the power condition is not savable.
		
		5 Timer Changeable
		     The Timer Changeable bit is valid if the Power Condition Supported bit is set to one, regardless of whether EPC is enabled or disabled. If the Timer Changeable bit is set to one, then the power condition is changeable if EPC is enabled. If the Timer Changeable bit is cleared to zero, then the power condition is not changeable.
		
		4 Default Timer Enabled
		     The Default Timer Enabled bit is valid if the Power Condition Supported bit is set to one, regardless of whether EPC is enabled or disabled.
		
		3 Saved Timer Enabled
		     The Saved Timer Enabled bit is valid if the Power Condition Supported bit is set to one, regardless of whether EPC is enabled or disabled.
		
		2 Current Timer Enabled
		     If EPC is disabled, then the Current Timer Enabled bit shall be cleared to zero. If EPC is enabled and the Current Timer Setting field is non-zero and the Current Timer Enabled bit is set to one, then the power condition timer is enabled. If EPC is enabled and the Current Timer Enabled bit is cleared to zero, then the power condition timer is disabled.
		
		1-0 Reserved

2-3	Byte	Reserved
4-7	DWord	Default Timer setting The Default Timer field is set at the time of manufacture. The Default Timer Setting field is valid if the Power Condition Supported bit is set to one, regardless of whether EPC is enabled or disabled. A value of FFFF_FFFFh indicates that the time is greater than or equal to 429_496_729_500 milliseconds. Measurement Units: 100 milliseconds.
8-11	DWord	Saved Timer setting The Saved Timer Setting field is a value that has been saved by a SET FEATURES Set Power Condition Timer subcommand. The Saved Timer Setting field is valid if the Power Condition Supported bit is set to one, regardless of whether EPC is enabled or disabled. A value of zero indicates that this power condition is disabled if the EPC feature set is enabled. A value of FFFF_FFFFh indicates that the time is greater than or equal to 429_496_729_500 milliseconds. Measurement Units: 100 milliseconds.

Table 131   Power Condition Log Description – Continued

Offset	Type	Description
12-15	DWord	Current Timer setting The Current Timer setting is the minimum time that the device shall wait after command completion before entering this power condition if the EPC feature set is enabled. The Current Timer Setting field shall be cleared to zero if: a) EPC is disabled; b) the Power Condition Supported bit is cleared to zero; or c) the Current Timer Enabled field is cleared to zero. A value of FFFF_FFFFh indicates that the time is greater than or equal to 429_496_729_500 milliseconds. Measurement Units: 100 milliseconds
16-19	DWord	Nominal Recovery time from to PM0:Active power management state The Nominal Recovery time from power to PM0: Active is the nominal time required to transition from power to PM0: Active power management state. This time does not include processing time for the command that caused this transition to occur. A value of zero indicates that the nominal recovery time is not specified. A value of FFFF_FFFFh indicates that the recovery time is greater than or equal to 429 496 729 500 milliseconds. Measurement Units: 100 milliseconds. This value is preserved over all resets.
20-23	DWord	Minimum timer setting The Minimum timer setting is the minimum timer value allowed by the Set Power Condition Timer subcommand for the timer. A value of zero indicates that the minimum timer value is not specified. A value of FFFF_FFFFh indicates that the minimum timer value is greater than or equal to 429 496 729 500 milliseconds. Measurement Units: 100 milliseconds This value be preserved over all resets
24-27	DWord	Maximum timer setting The Maximum timer setting is the maximum timer value allowed by the Set Power Condition Timer subcommand for the timer. A value of zero indicates that the maximum timer value is not specified. A value of FFFF_FFFFh indicates that the maximum timer value is greater than or equal to 429 496 729 500 milliseconds. Measurement Units: 100 milliseconds This value be preserved over all resets
28-63	DWord	Reserved

11.19.6 Queued Error Log

Table 132 defines the format of the Queued Error Log data structure.

Table 132 Queued Error Log Data Structure Definition

Byte	7	6	5	4	3	2		1	0
0	NQ	UNL	R				TAG		
1		Reserved							
2		Status(7:0)							
3		Error(7:0)							
4		LBA(7:0)							
5		LBA(15:8)							
6		LBA(23:16)							
7		Device(7:0)							
8		LBA(31:24)							
9		LBA(39:32)							
10		LBA(47:40)							
11		Reserved							
12		Count(7:0)							
13		Count(15:8)							
14		Sense Key							
15		Additional Sense Code							
16		Additional Sense Code Qualifier							
17		Final LBA In Error(7:0)							
18		Final LBA In Error(15:8)							
19		Final LBA In Error(23:16)							
20		Final LBA In Error(31:24)							
21		Final LBA In Error(39:32)							
22		Final LBA In Error(47:40)							
23 – 255		Reserved							
256 – 510		Vendor Unique							
511		Data Structure Checksum							

The TAG field (Byte 0 Bits 4-0) contains the tag number corresponding to a queued command if the NQ bit is cleared.

The NQ field (Byte 0 Bit 7) indicates whether the error condition was a result of a non-queued or not. If it is cleared the error information corresponds to a queued command specified by the tag number indicated in the TAG field.

The bytes 1 to 13 correspond to the contents of Shadow Register Block when the error was reported.

The Data Structure Checksum (Byte 511) contains the 2's complement of the sum of the first 511 bytes in the data structure. The sum of all 512 bytes of the data structure will be zero when the checksum is correct.

11.19.7 Identify Device Data Log (log page 30h)

IDENTIFY DEVICE data log reports device configuration information. This log is read-only. See table 99 for a list of defined pages. Each page consists of a header field that is followed by defined statistics fields. If the Revision Number field in the page header is 0000h, then that page is not supported. All page data following the last defined statistic for that page is reserved.

Table 133 Identify Device Data Log

Description	Page
List of supported pages	00h
Copy of IDENTIFY DEVICE data	01h
Capacity	02h
Supported Capabilities	03h
Current Settings	04h
ATA Strings	05h
Security	06h
Reserved for Parallel ATA	07h
Serial ATA	08h
Reserved	09h..FFh

11.19.7.1 List of Supported IDENTIFY DEVICE Data Log Pages (Page 00h)

IDENTIFY DEVICE data log page 00h contains a list of the supported pages. Entries are in order of ascending page number (e.g., 00h, 01h, 07h).

Table 134 List of Supported IDENTIFY DEVICE Data Pages

Offset	Type	Content	
0..7	QWord	IDENTIFY DEVICE data log Information Header. This log page lists the numbers of the supported log pages	
		Bit	**Meaning**
		63:24	Reserved
		23:16	Page Number. Set to 00h.
		15:0	Revision number. Set to 0001h
8	Byte	Number of entries (n) in the following list	
9	Byte	Set to zero to indicate that page 00h is supported	
10	Byte	Set to one to indicate that page 01h is supported	
		…	
n+8	Byte	Page number of nth supported IDENTIFY DEVICE data log page	
n+9..511		Reserved	

11.19.7.2 Copy of IDENTIFY DEVICE Data (log page 01h)

This page is a copy of IDENTIFY DEVICE data words 0..255.

11.19.7.3　Capacity (log page 02h)

The Capacity log page provides information about the capacity of the device.

Table 135　Capacity (Log Page 02h)

Offset	Type	Content
0..7	QWord	Capacity page information header
		Bit　　　**Meaning** 63　　　　Set to one. 62:24　　Reserved 23:16　　Page Number. Shall be set to 02h. 15:0　　　Revision number. Shall be set to 0001h
8..15	QWord	Device Capacity
		Bit　　　**Meaning** 63　　　　Set to one. 62:48　　Reserved 47:0　　　ACCESSIBLE CAPACITY field
16..23	QWord	Physical/Logical Sector Size
		Bit　　　**Meaning** 63　　　　Contents of the QWord are valid 62　　　　LOGICAL TO PHYSICAL SECTOR RELATIONSHIP SUPPORTED bit 61　　　　LOGICAL SECTOR SIZE SUPPORTED bit 60:22　　Reserved 21:20　　ALIGNMENT ERROR REPORTING field 19:16　　LOGICAL TO PHYSICAL SECTOR RELATIONSHIP field 15:0　　　LOGICAL SECTOR OFFSET field
24..31	QWord	Logical Sector Size
		Bit　　　**Meaning** 63　　　　Contents of the QWord are valid 62..32　　Reserved 31..0　　　LOGICAL SECTOR SIZE field
32..39	QWord	Nominal Buffer Size
		Bit　　　**Meaning** 63　　　　Contents of the QWord are valid 62:0　　　BUFFER SIZE field
40..511		Reserved

11.19.7.4   Supported Capabilities (log page 03h)

The Supported Capabilities log page provides a mechanism for the device to report support for feature sets, features, commands and other device capabilities.

Table 136   Supported Capabilities (Log Page 03h)

Offset	Type	Content
0..7	QWord	Supported Capabilities page information header.
		Bit **Meaning** 63 Set to one 62:24 Reserved 23:16 Page Number. Set to 03h 15:0 Revision number. Set to 0001h
8..15	QWord	Supported Capabilities
		Bit **Meaning** 63 Set to one 62:46 Reserved 49 SET SECTOR CONFIGURATION SUPPORTED bit 45 REQUEST SENSE DEVICE FAULT SUPPORTED bit 44 DSN SUPPORTED bit 43 LOW POWER STANDBY SUPPORTED bit 42 SET EPC POWER SOURCE SUPPORTED bit 41 AMAX ADDR SUPPORTED bit 40 Reserved for CFA 39 DRAT SUPPORTED bit 38 LPS MISALIGNMENT REPORTING SUPPORTED bit 37 Reserved 36 READ BUFFER DMA SUPPORTED bit 35 WRITE BUFFER DMA SUPPORTED bit 34 Reserved 33 DOWNLOAD MICROCODE DMA SUPPORTED bit 32 28-BIT SUPPORTED bit 31 RZAT SUPPORTED bit 30 Reserved 29 NOP SUPPORTED bit 28 READ BUFFER SUPPORTED bit 27 WRITE BUFFER SUPPORTED bit 26 Reserved 25 READ LOOK-AHEAD SUPPORTED bit 24 VOLATILE WRITE CACHE SUPPORTED bit 23 SMART bit 22 FLUSH CACHE EXT SUPPORTED bit 21 Reserved 20 48-BIT SUPPORTED bit 19 Reserved 18 SPIN-UP SUPPORTED bit 17 PUIS SUPPORTED bit 16 APM SUPPORTED bit 15 CFA SUPPORTED bit 14 DOWNLOAD MICROCODE SUPPORTED bit 13 UNLOAD SUPPORTED bit 12 The WRITE DMA FUA EXT and WRITE MULTIPLE FUA EXT commands are Supported

Table 137 Supported Capabilities (Log Page 03h) - Continued

Offset	Type	Content		
8..15	QWord	Supported Capabilities		
		11	GPL SUPPORTED bit	
		10	STREAMING SUPPORTED bit	
		9	Reserved	
		8	SMART SELF-TEST SUPPORTED bit	
		7	SMART ERROR LOGGING SUPPORTED bit	
		6	EPC SUPPORTED bit	
		5	SENSE DATA SUPPORTED bit	
		4	FREE-FALL SUPPORTED bit	
		3	DM MODE 3 SUPPORTED bit	
		2	GPL DMA SUPPORTED bit	
		1	WRITE UNCORRECTABLE SUPPORTED bit	
		0	WRV SUPPORTED bit	
16..23	QWord	DOWNLOAD MICROCODE Capabilities		
		Bit	**Meaning**	
		63	Contents of the QWord are valid	
		62:35	Reserved	
		34	DM OFFSETS DEFERRED SUPPORTED bit	
		33	DM IMMEDIATE SUPPORTED bit	
		32	DM OFFSETS IMMEDIATE SUPPORTED bit	
		31:16	DM MAXIMUM TRANSFER SIZE field	
		15:0	DM MINIMUM TRANSFER SIZE field	
24..31	QWord	Nominal Media Rotation Rate		
		Bit	**Meaning**	
		63	Set to one	
		62:16	Reserved	
		15:0	NOMINAL MEDIA ROTATION RATE field	
32..39	QWord	Nominal Form Factor [was word 168]		
		Bit	Meaning	
		63	Contents of the QWord are valid	
		62:4	Reserved	
		3:0	Nominal Form Factor	
40..47	QWord	Write-Read-Verify Sector Count Mode 3		
		Bit	**Meaning**	
		63	Contents of the QWord are valid	
		62:32	Reserved	
		31:0	WRV MODE 3 COUNT field	
48..55	QWord	Write-Read-Verify Sector Count Mode 2		
		Bit	**Meaning**	
		63	Contents of the QWord are valid	
		62:32	Reserved	
		31:0	WRV MODE 2 COUNT field	
56..71	DQWord	World wide name [was word 108]		
		Bit	**Meaning**	
		127	Set to one	
		126:64	Reserved	
		63:0	World wide name	

Table 138   Supported Capabilities log page - Continued

Offset	Type	Content
72..79	QWord	DATA SET MANAGEMENT **Bit** **Meaning** 63 Set to one 62:1 Reserved 0 TRIM SUPPORTED bit
80..511		Reserved

11.19.7.5   Current Settings (log page 04h)

The Current Settings log page provides a mechanism for the device to report the current settings for feature sets, features, and other device capabilities.

Table 139   Current Settings log page

Offset	Type	Content
0..7	QWord	Supported Capabilities page information header.
		Bit　　**Meaning** 63　　　Set to one 62:24　Reserved 23:16　Page Number. Set to 04h. 15:0　　Revision number. Set to 0001h
8..15	QWord	Current Settings
		Bit　　**Meaning** 63　　　Set to one 62:17　Reserved 16　　　DSN ENABLED bit 15　　　EPC ENABLED bit 14　　　8-BIT PIO ENABLED bit 13　　　VOLATILE WRITE CACHE ENABLED bit 12　　　Reserved for CFA 11　　　REVERTING TO DEFAULTS ENABLED bit 10　　　SENSE DATA ENABLED bit 9　　　Reserved 8　　　NON-VOLATILE WRITE CACHE bit 7　　　READ LOOK-AHEAD ENABLED bit 6　　　SMART ENABLED bit 5　　　Reserved 4　　　Reserved 3　　　PUIS ENABLED bit 2　　　APM ENABLED bit 1　　　FREE-FALL ENABLED bit 0　　　WRV ENABLED bit
16..23	QWord	Feature Settings
		Bit　　**Meaning** 63　　　Contents of the QWord are valid 62:16　Reserved 17:16　POWER SOURCE field 15:8　　APM LEVEL field 7:0　　　WRV MODE field
24..31	QWord	DMA Host Interface Sector Times
		Bit　　**Meaning** 63　　　Contents of the QWord are valid 62:16　Reserved 15:0　　DMA SECTOR TIME field
32..39	QWord	PIO Host Interface Sector Times
		Bit　　**Meaning** 63　　　Contents of the QWord are valid 62:16　Reserved 15:0　　PIO SECTOR TIME field

Table 140 Current Settings log page - Continued

Offset	Type	Content
40..47	QWord	Streaming minimum request size
		Bit **Meaning**
		63 Contents of the QWord are valid
		62:16 Reserved
		15:0 STREAM MIN REQUEST SIZE field
48..55	QWord	Streaming access latency
		Bit **Meaning**
		63 Contents of the QWord are valid
		62:16 Reserved
		15:0 STREAM ACCESS LATENCY field
56..63	QWord	Streaming Performance Granularity
		Bit **Meaning**
		63 Contents of the QWord are valid
		62:32 Reserved
		31:0 STREAM GRANULARITY field
64..71	QWord	Free-fall Control Sensitivity
		Bit **Meaning**
		63 Contents of the QWord are valid
		62:16 Reserved
		7:0 FREE-FALL SENSITIVITY field
72..79	QWord	Device Maintenance Schedule
		Bit **Meaning**
		63 Contents of the QWord are valid
		62:48 Reserved
		47:32 Time scheduled for device maintenance
		31:16 Time to performance degradation
		15:0 Minimum inactive time
80..511		Reserved

11.19.7.6 Strings (log page 05h)

The Strings log page provides a mechanism for the device to report ATA String based information.

Table 141 Strings (Log Page 05h)

Offset	Type	Content
0..7	QWord	Strings page information header.
		Bit **Meaning**
		63 Set to one
		62:24 Reserved
		23:16 Page Number. Set to 05h
		15:0 Revision number. Set to 0001h
8..27	ATA String	Serial number
28..31		Reserved
32..39	ATA String	Firmware revision
40..47		Reserved
48..87	ATA String	Model number
88..95		Reserved
96..103	ATA String	Additional Product Identifier
104..511		Reserved

11.19.7.7 Security (log page 06h)

The Security log page provides a mechanism for the device to report Security based information.

Table 142 Security (Log Page 06h)

Offset	Type	Content
0..7	QWord	Security page information header.
		Bit **Meaning** 63 Set to one 62:24 Reserved 23:16 Page Number. Set to 06h. 15:0 Revision number. Set to 0001h
8..15	QWord	Master Password Identifier [was word 92]
		Bit **Meaning** 63 Contents of the QWord are valid. 62:16 Reserved 15:0 Master Password Identifier
16..23	QWord	Security Status
		Bit **Meaning** 63 Contents of the QWord are valid 62:7 Reserved 6 SECURITY SUPPORTED bit 5 MASTER PASSWORD CAPABILITY bit 4 ENHANCED SECURITY ERASE SUPPORTED bit 3 SECURITY COUNT EXPIRED bit 2 SECURITY FROZEN bit 1 SECURITY LOCKED bit 0 SECURITY ENABLED bit
24..31	QWord	Time required for an Enhanced Erase mode SECURITY ERASE UNIT command [was word 90]
		Bit **Meaning** 63 Contents of the QWord are valid 62:15 Reserved 14:0 ENHANCED SECURITY ERASE TIME field
32..39	QWord	Time required for a Normal Erase mode SECURITY ERASE UNIT command [was word 89]
		Bit **Meaning** 63 Contents of the QWord are valid 62:15 Reserved 14:0 NORMAL SECURITY ERASE TIME field
40..47	QWord	Trusted Computing feature set
		Bit **Meaning** 63 Contents of the QWord are valid 62:1 Reserved 0 TRUSTED COMPUTING SUPPORTED bit
		4 BLOCK ERASE SUPPORTED bit 3 OVERWRITE SUPPORTED bit 1 SANITIZE SUPPORTED bit 0 ENCRYPT ALL SUPPORTED bit

Table 143 Security (Log Page 06h) - Continued

Offset	Type	Content	
48..55	QWord	Security Capabilities	
		Bit	**Meaning**
		63	Contents of the QWord are valid
		62:8	Reserved
		7	RESTRICTED SANITIZE OVERRIDES SECURITY bit
		6	ACS-3 COMMANDS ALLOWED BY SANITIZE bit
		5	SANITIZE ANTIFREEZE LOCK SUPPORTED bit
		4	BLOCK ERASE SUPPORTED bit
		3	OVERWRITE SUPPORTED bit
		1	SANITIZE SUPPORTED bit
		0	ENCRYPT ALL SUPPORTED bit
56..511		Reserved	

11.19.7.8 Parallel ATA (log page 07h)

The Parallel ATA log page provides information about the Parallel ATA Transport.   This page is not supported.

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11.19.7.9   Serial ATA (log page 08h)

The Serial ATA log page provides information about the Serial ATA Transport.

Table 144   Serial ATA (Log Page 08h)

Offset	Type	Content
0..7	QWord	Serial ATA page information header. **Bit**　**Meaning** 63　　Set to one 62:24　Reserved 23:16　Page Number. Set to 08h. 15:0　　Revision number. Set to 0001h
8..15	QWord	SATA Capabilities **Bit**　**Meaning** 63　　Set to one 62:29　Reserved for Serial ATA 28　　DIPM SSP PRESERVATION SUPPORTED 27　　Reserved 26　　DEVSLEEP_TO_REDUCEDPWRSTATE CAPABILITY SUPPORTED 25　　DEVICE SLEEP SUPPORTED 24　　NCQ AUTOSENSE SUPPORTED bit 23　　SOFTWARE SETTINGS PRESERVATION SUPPORTED bit 22　　HARDWARE FEATURE CONTROL SUPPORTED bit 21　　IN-ORDER DATA DELIVERY SUPPORTED bit 20　　DEVICE INITIATED POWER MANAGEMENT SUPPORTED bit 19　　DMA SETUP AUTO-ACTIVATION SUPPORTED bit 18　　NON-ZERO BUFFER OFFSETS SUPPORTED bit 17　　SEND AND RECEIVE QUEUED COMMANDS SUPPORTED bit 16　　NCQ NON-DATA COMMAND SUPPORTED bit 15　　NCQ STREAMING SUPPORTED bit 14　　READ LOG DMA EXT AS EQUIVALENT TO READ LOG EXT SUPPORTED bit 13　　DEVICE AUTOMATIC PARTIAL TO SLUMBER TRANSITIONS SUPPORTED bit 12　　HOST AUTOMATIC PARTIAL TO SLUMBER TRANSITIONS SUPPORTED bit 11　　NCQ PRIORITY INFORMATION SUPPORTED bit 10　　UNLOAD WHILE NCQ COMMANDS ARE OUTSTANDING SUPPORTED bit 9　　SATA PHY EVENT COUNTERS LOG SUPPORTED bit 8　　RECEIPT OF HOST INITIATED POWER MANAGEMENT REQUESTS SUPPORTED bit 7　　NCQ FEATURE SET SUPPORTED bit 6:3　　Reserved 2　　SATA GEN3 SIGNALING SPEED SUPPORTED bit 1　　SATA GEN2 SIGNALING SPEED SUPPORTED bit 0　　SATA GEN1 SIGNALING SPEED SUPPORTED bit

Table 145 Serial ATA (Log Page 08h)- Continued

Offset	Type	Content
16..23	QWord	Current SATA Settings **Bit** **Meaning** 63 Set to one 62:11 Reserved 10 DEVICE SLEEP ENABLED bit 9 AUTOMATIC PARTIAL TO SLUMBER TRANSITIONS ENABLED bit 8 SOFTWARE SETTINGS PRESERVATION ENABLED bit 7 HARDWARE FEATURE CONTROL IS ENABLED bit 6 IN-ORDER DATA DELIVERY ENABLED bit 5 DEVICE INITIATED POWER MANAGEMENT ENABLED bit) 4 DMA SETUP AUTO-ACTIVATION ENABLED bit 3 NON-ZERO BUFFER OFFSETS ENABLED bit 2:0 CURRENT SERIAL ATA SIGNAL SPEED field
24..39		Reserved
40..41	Word	CURRENT HARDWARE FEATURE CONTROL IDENTIFIER field
42..43	Word	SUPPORTED HARDWARE FEATURE CONTROL IDENTIFIER field
44..47		Reserved
48..55	QWord	DEVSLP TIMING VARIABLES **Bit** **Meaning** 63 DEVSLP SUPPORTED 62:16 Reserved 15:8 DEVSLEEP EXIT TIMEOUT (DETO) 7:5 Reserved 4:0 MINIMUM DEVSLP ASSERTION TIME (MDAT)
56..63	QWord	TRANSITIONAL ENERGY REPORTING **Bit** **Meaning** 63 TER SUPPORTED 62:55 Reserved 54:53 IN-STATE DEVSLEEP POWER UNIT 52:48 TYPICAL IN-STATE DEVSLEEP POWER 47:46 OFF TO GOOD STS LATENCY TIME UNIT 45:40 OFF TO GOOD STS LATENCY 39:38 BETWEEN POWER CYCLES TIME UNIT 37:24 RECOMMENDED TIME BETWEEN POWER CYCLES 23:22 OFF TO GOOD STS TIME UNIT 21:16 OFF TO GOOD STS RECOUP COST 15:14 DEVSLEEP TO PHYRDY TIME UNIT 13:8 DEVSLEEP TO PHYRDY RECOUP COST 7:6 SLUMBER TO DEVSLEEP TIME UNIT 5:0 SLUMBER TO DEVSLEEP RECOUP COST

Table 146   Serial ATA (Log Page 08h)- Continued

Offset	Type	Content
64..71	QWord	TRANSITIONAL ENERGY REPORTING EXTENDED **Bit** **Meaning** 63 TERE SUPPORTED 62:47 Reserved 46:45 IN-STATE SLUMBER POWER UNITS 44:40 TYPICAL IN-STATE SLUMBER POWER 39:38 PM2 TO PM0 LATENCY TIME UNIT 37:32 PM2 TO PM0 LATENCY 31:30 OFF TO GOOD STS RELATIVE TO DEVSLEEP/PM2 TIME UNIT 29:24 OFF TO GOOD STS RELATIVE TO DEVSLEEP/PM2 RECOUP COST 23:22 DEVSLEEP/PM2 TO OFF TIME UNIT 21:16 DEVSLEEP/PM2 TO OFF RECOUP COST 15:14 PM2 TO PM0 TIME UNIT 13:8 PM2 TO PM0 RECOUP COST 7:6 PM0 TO PM2 TIME UNIT 5:0 PM0 TO PM2 RECOUP COST
72..511		Reserved

11.20 Read Log DMA Ext (47h)

The content of this command is the same as Read Log Ext. See Section 11.19 Read Log Ext (2fh).

Table 147   Read Log DMA Ext Command (47h)

Command Block Output Registers		7	6	5	4	3	2	1	0
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Feature	Current	-	-	-	-	-	-	-	R-
	Previous	-	-	-	-	-	-	-	-
Sector Count	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
LBA Low	Current	V	V	V	V	V	V	V	V
	Previous	-	-	-	-	-	-	-	-
LBA Mid	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
LBA High	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Device		-	-	-	-	-	-	-	-
Command		0	1	0	0	0	1	1	1

Command Block Input Registers		7	6	5	4	3	2	1	0
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Error					...See Below...				
Sector Count	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
LBA Low	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
LBA Mid	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
LBA High	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Device		-	-	-	-	-	-	-	-
Status					...See Below...				

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
V	V	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	0	V

Normal Outputs

See Normal Outputs in Section 11.6 "*Flush Cache Ext (EAh)"*

Error Outputs

See Error Outputs in Section 11.19 "**Error! Reference source not found.**"

11.21   Read Multiple (C4h)

The Read Multiple command reads one or more sectors of data from disk media, and then transfers the data from the device to the host.

The sectors are transferred through the Data Register 16 bits at a time. Command execution is identical to the Read Sector(s) command except that an interrupt is generated for each block (as defined by the Set Multiple command) instead of for each sector.

Table 148   Read Multiple Commands (C4h)

Command Block Output Registers										Command Block Input Registers									
Register	7	6	5	4	3	2	1	0		Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-		Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-		Error			…See Below…					
Sector Count	V	V	V	V	V	V	V	V		Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V		Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V		Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V		Cylinder High	V	V	V	V	V	V	V	V
Device/Head	1	L	1	D	H	H	H	H		Device/Head	-	-	-	-	H	H	H	H
Command	1	1	0	0	0	1	0	0		Status			…See Below…					

Error Register								Status Register							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN	BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	0	V	0	0	0	V	0	V	-	0	-	V

Normal Outputs

See Normal Outputs in *Section 11.5 "Flush Cache (E7h)"*

Error Outputs

See Error Outputs in *Section 11.6 "Read DMA (C8h/C9h)"*

11.22   Read Multiple Ext (29h)

The Read Multiple Ext command reads one or more sectors of data from disk media, and then transfers the data from the device to the host.

The sectors are transferred through the Data Register 16 bits at a time. Command execution is identical to the Read Sector(s) command except that an interrupt is generated for each block (as defined by the Set Multiple command) instead of for each sector.

Table 149   Read Multiple Ext Command (29h)

Command Block Output Registers		7	6	5	4	3	2	1	0
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Feature	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Sector Count	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Sector Number	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder Low	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder High	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Device/Head		-	1	-	D	-	-	-	-
Command		0	0	1	0	1	0	0	1

Command Block Input Registers		7	6	5	4	3	2	1	0
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Error		…See Below…							
Sector Count	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Sector Number	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Cylinder Low	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Cylinder High	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Device/Head		-	-	-	-	-	-	-	-
Status		…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	V	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Output Parameters To The Device

Sector Count Current The number of continuous sectors to be transferred low order, bits (7:0).

Sector Count Previous The number of continuous sectors to be transferred high order, bits (15:8).   If 0000h is specified in the Sector Count register, then 65,536 sectors will be transferred.

Sector Number Current LBA (7:0).

Sector Number Previous LBA (31:24).

Cylinder Low Current LBA (15:8).

Cylinder Low Previous LBA (39:32).

Cylinder High Current LBA (23:16).

Cylinder High Previous LBA (47:40).

Input Parameters From The Device

Sector Number (HOB=0) LBA (7:0) of the address of the first unrecoverable error.

Sector Number (HOB=1) LBA (31:24) of the address of the first unrecoverable error.

Cylinder Low (HOB=0) LBA (15:8) of the address of the first unrecoverable error.

Cylinder Low (HOB=1) LBA (39:32) of the address of the first unrecoverable error.

Cylinder High (HOB=0) LBA (23:16) of the address of the first unrecoverable error.

Cylinder High (HOB=1) LBA (47:40) of the address of the first unrecoverable error.

11.23   Read Sector(s) (20h)

The Read Sector(s) command reads one or more sectors of data from disk media, and then transfers the data from the device to the host.

The sectors are transferred through the Data Register 16 bits at a time.

If an uncorrectable error occurs, the read will be terminated at the failing sector.

Table 150   Read Sector(s) Command (20h)

Command Block Output Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	1	L	1	D	H	H	H	H
Command	0	0	1	0	0	0	0	R

Command Block Input Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below…							
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	-	-	-	-	H	H	H	H
Status	…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	V	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Output Parameters To The Device

Sector Count	The number of continuous sectors to be transferred. If zero is specified, then 256 sectors will be transferred.
Sector Number	The sector number of the first sector to be transferred. (L=0) In LBA mode, this register contains LBA bits 0 – 7. (L=1)
Cylinder High/Low	The cylinder number of the first sector to be transferred. (L=0) In LBA mode, this register contains LBA bits 8 – 15 (Low), 16 – 23 (High). (L=1)
H	The head number of the first sector to be transferred. (L=0) In LBA mode, this register contains LBA bits 24 – 27. (L=1)
R	The retry bit, but this bit is ignored.

Input Parameters From The Device

Sector Count	The number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs.
Sector Number	The sector number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 0 – 7. (L=1)
Cylinder High/Low	The cylinder number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 8 – 15 (Low), 16 – 23 (High). (L=1)
H	The head number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 24 – 27. (L=1)

11.24   Read Sector(s) Ext (24h)

The Read Sector(s) Ext command reads from 1 to 65,536 sectors of data from disk media, and then transfers the data from the device to the host.

The sectors are transferred through the Data Register 16 bits at a time.

If an uncorrectable error occurs, the read will be terminated at the failing sector

Table 151   Read Sector(s) Ext Command (24h)

Command Block Output Registers		7	6	5	4	3	2	1	0
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Feature	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Sector Count	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Sector Number	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder Low	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder High	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Device/Head		1	1	1	D	-	-	-	-
Command		0	0	1	0	0	1	0	0

Command Block Input Registers		7	6	5	4	3	2	1	0
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Error		…See Below…							
Sector Count	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Sector Number	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Cylinder Low	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Cylinder High	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Device/Head		-	-	-	-	-	-	-	-
Status		…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	V	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Output Parameters To The Device

Sector Count Current	The number of continuous sectors to be transferred low order, bits (7:0)
Sector Count Previous	The number of continuous sectors to be transferred high order, bits (15:8). If zero is specified in the Sector Count register, then 65,536 sectors will be transferred.
Sector Number Current	LBA (7:0).
Sector Number Previous	LBA (31:24).
Cylinder Low Current	LBA (15:8).
Cylinder Low Previous	LBA (39:32).
Cylinder High Current	LBA (23:16).
Cylinder High Previous	LBA (47:40).

Input Parameters From The Device

Sector Number (HOB=0)	LBA (7:0) of the address of the first unrecoverable error.
Sector Number (HOB=1)	LBA (31:24) of the address of the first unrecoverable error.
Cylinder Low (HOB=0)	LBA (15:8) of the address of the first unrecoverable error.
Cylinder Low (HOB=1)	LBA (39:32) of the address of the first unrecoverable error.
Cylinder High (HOB=0)	LBA (23:16) of the address of the first unrecoverable error.
Cylinder High (HOB=1)	LBA (47:40) of the address of the first unrecoverable error.

11.25 Read Verify Sector(s) (40h/41h)

The Read Verify Sector(s) verifies one or more sectors on the device. No data is transferred to the host.

The difference between Read Sector(s) command and Read Verify Sector(s) command is whether the data is transferred to the host or not.

If an uncorrectable error occurs, the read verify will be terminated at the failing sector.

Table 152 Read Verify Sector(s) Command (40h/41h)

Command Block Output Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	1	L	1	D	H	H	H	H
Command	0	0	1	0	0	0	0	R

Command Block Input Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below…							
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	-	-	-	-	H	H	H	H
Status	…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	V	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Output Parameters To The Device

Sector Count	The number of continuous sectors to be verified. If zero is specified, then 256 sectors will be verified.
Sector Number	The sector number of the first sector to be transferred. (L=0) In LBA mode, this register contains LBA bits 0 – 7. (L=1)
Cylinder High/Low	The cylinder number of the first sector to be transferred. (L=0) In LBA mode, this register contains LBA bits 8 – 15 (Low), 16 – 23 (High). (L=1)
H	The head number of the first sector to be transferred. (L=0) In LBA mode, this register contains LBA bits 24 – 27. (L=1)
R	The retry bit, but this bit is ignored.

Input Parameters From The Device

Sector Count	The number of requested sectors not verified. This will be zero, unless an unrecoverable error occurs.
Sector Number	The sector number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 0 – 7. (L=1)
Cylinder High/Low	The cylinder number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 8 – 15 (Low), 16 – 23 (High). (L=1)
H	The head number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 24 – 27. (L=1)

11.26   Read Verify Sector(s) Ext (42h)

The Read Verify Sector(s) Ext verifies one or more sectors on the device. No data is transferred to the host.

The difference between the Read Sector(s) Ext command and the Read Verify Sector(s) Ext command is whether the data is transferred to the host or not.

If an uncorrectable error occurs, the Read Verify Sector(s) Ext will be terminated at the failing sector.

Table 153   Read Verify Sector(s) Ext Command (42h)

Command Block Output Registers		7	6	5	4	3	2	1	0
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Feature	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Sector Count	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Sector Number	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder Low	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder High	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Device/Head		1	1	1	D	-	-	-	-
Command		0	0	1	0	0	0	1	0

Command Block Input Registers		7	6	5	4	3	2	1	0
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Error		…See Below…							
Sector Count	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Sector Number	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Cylinder Low	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Cylinder High	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Device/Head		-	-	-	-	-	-	-	-
Status		…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	V	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Output Parameters To The Device

Sector Count Current	The number of continuous sectors to be verified low order, bits (7:0).
Sector Count Previous	The number of continuous sectors to be verified high order, bits (15:8). If zero is specified in the Sector Count register, then 65,536 sectors will be verified.
Sector Number Current	LBA (7:0).
Sector Number Previous	LBA (31:24)
Cylinder Low Current	LBA (15:8).
Cylinder Low Previous	LBA (39:32).
Cylinder High Current	LBA (23:16).
Cylinder High Previous	LBA (47:40).

Input Parameters From The Device

Sector Number (HOB=0)	LBA (7:0) of the address of the first unrecoverable error.
Sector Number (HOB=1)	LBA (31:24) of the address of the first unrecoverable error.
Cylinder Low (HOB=0)	LBA (15:8) of the address of the first unrecoverable error.
Cylinder Low (HOB=1)	LBA (39:32) of the address of the first unrecoverable error.
Cylinder High (HOB=0)	LBA (23:16) of the address of the first unrecoverable error.
Cylinder High (HOB=1)	LBA (47:40) of the address of the first unrecoverable error.

11.27 Recalibrate (1xh)

The Recalibrate command moves the read/write heads from anywhere on the disk to cylinder 0.

If the device cannot reach cylinder 0, T0N (Track 0 Not Found) will be set in the Error Register.

Table 154 Recalibrate Command (1xh)

Command Block Output Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	0	0	0	1	-	-	-	-

Command Block Input Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below…							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	V	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

11.28 Request Sense Data Ext (0Bh)

The Request Sense Data Ext command allows the reporting of the most recent sense data from the device.
When sense data is available, the sense key (K), additional sense code (C), and additional sense code qualifier (Q) fields shall be set to values that are defined in the SPC-4 standard.

Otherwise, the sense key, additional sense code, and additional sense code qualifier shall be cleared to zero.

Default of Sense Data Reporting feature set is invalid.

Request Sense Data Ext returns KCQ of the latest command execution result except C3 Command. KCQ is deleted after Request Sense Data Ext execution.

If another command is executed before Request Sense Data Ext execution, KCQ will be overwritten at the result of another command.

Request Sense Data Ext is not dependent on a setup of NCQ Auto Sense.

Request Sense Data Ext returns KCQ of Error which occurred in NCQ Command.

In Error of the command Aborted in the state of CA, KCQ of Error which occurred in NCQ Command is not updated.

Error of Non NCQ Command can perform acquisition of Sense Data in Read Log Ext (Page = 10h).

However, if Request Sense Data Ext is performed before Read Log Ext execution, Sense Data will become invalid, and the contents of Sense Data acquired by Read Log Ext are not guaranteed.

Table 155   Request Sense Data Ext Command (0Bh)

Command Block Output Registers		7	6	5	4	3	2	1	0
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Feature	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Sector Count	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Sector Number	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Cylinder Low	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Cylinder High	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Device/Head		1	1	1	D	-	-	-	-
Command		0	0	0	0	1	0	1	1

Command Block Input Registers		7	6	5	4	3	2	1	0
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Error		...See Below...							
Sector Count	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Sector Number	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	-	-	-	-	-	-	-	-
Cylinder Low	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	-	-	-	-	-	-	-	-
Cylinder High	HOB=0	-	-	-	-	V	V	V	V
	HOB=1	-	-	-	-	-	-	-	-
Device/Head		-	-	-	-	-	-	-	-
Status		...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	V	V

About Status Register bit 1(Sense Data Available)

The Sense Data Available bit shall be set to one if:
   a) IDENTIFY DEVICE data word 119 bit 6 is set to one;
   b) IDENTIFY DEVICE data word 120 bit 6 is set to one; and
   c) Device has sense data to report after processing any command.

The Error bit and the Sense Data Available may both be set to one.

Bit 1 of the Status Register is obsolete if:

a) IDENTIFY DEVICE data word 119 bit 6 is cleared to zero; or

b) IDENTIFY DEVICE data word 120 bit 6 is cleared to zero.

Table 156   Sanitize Device Feature Set (B4h)

Input Parameters From The Device	
Sector Number (HOB=0)	Additional Sense Code Qualifier (Bit 7:0)
Cylinder Low (HOB=0)	Additional Sense Code (Bit 15:8)
Cylinder High (HOB=0)	Sense Key (Bit 19:16)

11.28.1   Overwrite Ext Command (Feature: 0014h)

Table 157   Overwrite Ext Command (B4h/0014h)

Command Block Output Registers		7	6	5	4	3	2	1	0
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Feature	Current	0	0	0	1	0	1	0	0
	Previous	0	0	0	0	0	0	0	0
Sector Count	Current	V	-	-	V	V	V	V	V
	Previous	-	-	-	-	-	-	-	-
Sector Number	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder Low	Current	V	V	V	V	V	V	V	V
	Previous	0	1	0	1	0	1	1	1
Cylinder High	Current	V	V	V	V	V	V	V	V
	Previous	0	1	0	0	1	1	1	1
Device/Head		1	1	1	D	-	-	-	-
Command		1	0	1	1	0	1	0	1

Command Block Input Registers		7	6	5	4	3	2	1	0
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Error		...See Below...							
Sector Count	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	V	V	V	-	-	-	-	-
Sector Number	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	-	-	-	-	-	-	-	-
Cylinder Low	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	-	-	-	-	-	-	-	-
Cylinder High	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Device/Head		-	-	-	-	-	-	-	-
Status		...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
V	Vs	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

The OVERWRITE EXT command starts an overwrite operation (i.e., a sanitize operation on the internal media that stores user data) which fills the user data area with a four byte pattern specified in the LBA field of the command. Parameters for the OVERWRITE EXT command include a count for multiple overwrites and the option to invert the four byte pattern between consecutive overwrite passes.

After the overwrite operation has been successfully applied, affected data blocks are readable without error.

The OVERWRITE EXT command only is processed if:

a)   the Sanitize Device feature set is supported

b)   the device is in the SD0: Sanitize Idle state, the SD3: Sanitize Operation Failed state, or the SD4: Sanitize Operation Succeeded state.

Output Parameters To The Device

Sector Count Current bit 7	Invert pattern between overwrite operations
Sector Count Current bit 4	The FAILURE MODE
	1: the device may exit the SD3: Sanitize Operation Failed state with successful processing of a SANITIZE STATUS EXT command.
	0: the SD3: Sanitize Operation Failed state returns command aborted for sanitize operations with the FAILURE MODE bit set to one until the device returns to the SD1: Sanitize Idle state.
Sector Count Current bit 3:0	OVERWRITE OPERATION COUNT
	This specifies how many write operations occur in the overwrite operation. A count of zero requests sixteen write operations.
Sector Number Previous	OVERWRITE PATTERN (31:24)
	The OVERWRITE PATTERN specifies a DWord pattern to be written across each physical sector affected by this command.
Cylinder High Current	OVERWRITE PATTERN (23:16). Ditto.
Cylinder Low Current	OVERWRITE PATTERN (15:8). Ditto.
Sector Number Current	OVERWRITE PATTERN (7:0). Ditto.

Input Parameters From The Device

Sector Count Current bit 15	Sanitize Operation Completed Without Error.
	1: the Sanitize Device state machine enters SD4: Sanitize Operation Succeeded.
	0: the Sanitize Device state machine enters SD2: Sanitize Operation. The value of this bit is maintained across power-on resets.
Sector Count Current bit 14	Sanitize operation in progress
Sector Count Current bit 13	Device is in the SD1: Sanitize Frozen state
Cylinder Low (HOB=0)	The Sanitize Progress Indication (15:8).
	Progress indicator for the current sanitizes operation when the Sanitize Device state machine is in the SD2: Sanitize Operation state. This value is FFFFh if the Sanitize Device state machine is not in the SD2: Sanitize Operation state (i.e., a sanitize operation is not in process). The returned value is a numerator that has 65536 (10000h) as its denominator.
Sector Number (HOB=0)	The Sanitize Progress Indication (7:0). Ditto.

Error Output

The ABORT bit is set to one if a SANITIZE DEVICE FREEZE LOCK EXT command has successfully completed since the last power-on reset.

The device returns command aborted if:

a)   the device is in the SD3:Sanitize Operation Failed state

b)   the completed sanitize command (i.e. OVERWRITE EXT) contained the FAILURE MODE bit cleared to zero

c)   an OVERWRITE EXT command with the FAILURE MODE bit set to one is received.

Sector Number (HOB=0)	Sanitize Device Error (7:0)
	00h Reason not reported
	01h Sanitize Command Unsuccessful. The sanitize operation completed with physical sectors that are available to be allocated for user data that were not successfully sanitized.
	02h Invalid or unsupported Sanitize Device Feature Field Value
	03h Device is in the Sanitize Frozen state
	04h..FFh Reserved

11.28.2 Sanitize Freeze Lock Ext Command (Feature: 0020h)

The SANITIZE FREEZE LOCK EXT command sets the Sanitize Device state machine to the SD1: Sanitize Frozen state. After command completion all sanitize commands other than SANITIZE STATUS EXT command returns command aborted. The Sanitize Device state machine transitions from the SD1: Sanitize Frozen state to the SD0: Sanitize Idle state after a power-on reset or hardware reset.

Table 158 Sanitize Freeze Lock Ext Command (B4h/0020h)

Command Block Output Registers		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Feature	Current	0	0	1	0	0	0	0	0
	Previous	0	0	0	0	0	0	0	0
Sector Count	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Sector Number	Current	0	1	1	0	1	0	1	1
	Previous	0	1	0	0	0	1	1	0
Cylinder Low	Current	0	1	0	0	1	1	0	0
	Previous	-	-	-	-	-	-	-	-
Cylinder High	Current	0	1	1	1	0	0	1	0
	Previous	-	-	-	-	-	-	-	-
Device/Head		1	1	1	D	-	-	-	-
Command		1	0	1	1	0	1	0	1

Command Block Input Registers		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Error					...See Below...				
Sector Count	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	V	V	V	-	-	-	-	-
Sector Number	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	-	-	-	-	-	-	-	-
Cylinder Low	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	-	-	-	-	-	-	-	-
Cylinder High	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Device/Head		-	-	-	-	-	-	-	-
Status					...See Below...				

Error Register								
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
V	Vs	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Input Parameters From The Device

Sector Count Current bit 15 Sanitize Operation Completed Without Error.
  1: the Sanitize Device state machine enters SD4: Sanitize Operation Succeeded.
  0: the Sanitize Device state machine enters SD2: Sanitize Operation. The value of this bit is maintained across power-on resets.

Sector Count Current bit 14 Sanitize operation in progress

Sector Count Current bit 13 Device is in the SD1: Sanitize Frozen state

Cylinder Low (HOB=0) The Sanitize Progress Indication (15:8).
Progress indicator for the current sanitizes operation when the Sanitize Device state machine is in the SD2: Sanitize Operation state. This value is FFFFh if the Sanitize Device state machine is not in the
SD2: Sanitize Operation state (i.e., a sanitize operation is not in process). The returned value is a numerator that has 65536 (10000h) as its denominator.

Sector Number (HOB=0) The Sanitize Progress Indication (7:0). Ditto.

Error Output
Sector Number (HOB=0)   Sanitize Device Error (7:0)

           00h Reason not reported

           01h Sanitize Command Unsuccessful. The sanitize operation completed with physical sectors that are available to be allocated for user data that were not successfully sanitized.

           02h Invalid or unsupported Sanitize Device Feature Field Value

           03h Device is in the Sanitize Frozen state

           04h..FFh Reserved

11.28.3 Sanitize Status Ext Command (Feature: 0000h)

Table 159   Sanitize Status Ext Command (B4h/0000h)

Command Block Output Registers		7	6	5	4	3	2	1	0
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Feature	Current	0	0	0	0	0	0	0	0
	Previous	0	0	0	0	0	0	0	0
Sector Count	Current	-	-	-	-	-	-	-	V
	Previous	-	-	-	-	-	-	-	-
Sector Number	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Cylinder Low	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Cylinder High	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Device/Head		1	1	1	D	-	-	-	-
Command		1	0	1	1	0	1	0	1

Command Block Input Registers		7	6	5	4	3	2	1	0
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Error				...See Below...					
Sector Count	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	V	V	V	-	-	-	-	-
Sector Number	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	-	-	-	-	-	-	-	-
Cylinder Low	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	-	-	-	-	-	-	-	-
Cylinder High	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Device/Head		-	-	-	-	-	-	-	-
Status				...See Below...					

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
V	Vs	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

The SANITIZE STATUS EXT command returns information about current or previously completed sanitizes operations. This includes:

a)   progress indication on a current sanitize operation

b)   whether a previous sanitize operation completed successfully or unsuccessfully

c)   if an unsupported sanitize device command was received.

The SANITIZE STATUS EXT command is valid in every state of the Sanitize Device state machine.

Output Parameters To The Device

Sector Count Current bit 0   CLEAR SANITIZE OPERATION FAILED

If Sanitize Device state machine is in the SD3: Sanitize Failed state:

a)   the FAILURE MODE bit was set to one in the Sanitize Device command that caused the sanitize operation

b)   the sanitize operation failed

c)   the CLEAR SANITIZE OPERATION FAILED bit is set to one in the SANITIZE STATUS EXT command then the Sanitize Device state machine transitions to the SD0: Sanitize Idle state.

If the CLEAR SANITIZE OPERATION FAILED bit is set to one in the SANITIZE STATUS EXT command, and the FAILURE MODE bit was set to zero in the Sanitize Device command that caused the sanitize operation, the SANITIZE STATUS EXT command returns command aborted.

Input Parameters From The Device

Sector Count Current bit 15	Sanitize Operation Completed Without Error.

> 1: the Sanitize Device state machine enters SD4: Sanitize Operation Succeeded.
>
> 0: the Sanitize Device state machine enters SD2: Sanitize Operation. The value of this bit is maintained across power-on resets.

Sector Count Current bit 14	Sanitize operation in progress
Sector Count Current bit 13	Device is in the SD1: Sanitize Frozen state
Cylinder Low (HOB=0)	The Sanitize Progress Indication (15:8). Progress indicator for the current sanitizes operation when the Sanitize Device state machine is in the SD2: Sanitize Operation state. This value is FFFFh if the Sanitize Device state machine is not in the SD2: Sanitize Operation state (i.e., a sanitize operation is not in process). The returned value is a numerator that has 65536 (10000h) as its denominator.
Sector Number (HOB=0)	The Sanitize Progress Indication (7:0). Ditto.

Error Output

After the sanitize operation has completed, if any physical sector that is available to be allocated for user data was not successfully sanitized, then this command returns the ABORT bit set to one.

Sector Number (HOB=0)	Sanitize Device Error (7:0)

> 00h Reason not reported
>
> 01h Sanitize Command Unsuccessful. The sanitize operation completed with physical sectors that are available to be allocated for user data that were not successfully sanitized.
>
> 02h Invalid or unsupported Sanitize Device Feature Field Value
>
> 03h Device is in the Sanitize Frozen state
>
> 04h..FFh Reserved

11.29   Security Disable Password (F6h)

The Security Disable Password command disables the security mode feature (device lock function).

The Security Disable Password command requests a transfer of a single sector of data from the host including information specified in Table 192 on the page 233. Then the device checks the transferred password. If the User Password or Master Password matches the given password, the device disables the security mode feature (device lock function). This command does not change the Master Password which may be re-activated later by setting User Password. This command should be executed in device unlock mode.

When security is disabled and the Identifier bit is set to User, then the device shall return command aborted.

Table 160   Security Disable Password Command (F6h)

Command Block Output Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	1	0	1	1	0

Command Block Input Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below…							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	…See Below…							

Error Register								
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register								
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Table 161   Password Information for Security Disable Password command

Word	Description
00	Control word bit 0 : Identifier (1-Mater, 0-User) bit 1-15 : Reserved
01-16	Password (32 bytes)
17-255	Reserved

The device will compare the password sent from this host with that specified in the control word.

Identifier   Zero indicates that the device should check the supplied password against the user password stored internally. One indicates that the device should check the given password against the master password stored internally.

11.30   Security Erase Prepare (F3h)

The Security Erase Prepare Command must be issued immediately before the Security Erase Unit Command to enable device erasing and unlocking.

This command does not request to transfer data.

Table 162   Security Erase Prepare Command (F3h)

Command Block Output Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	1	0	0	1	1

Command Block Input Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below…							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

11.31 Security Erase Unit (F4h)

The Security Erase Unit command initializes all user data sectors, and then disables the device lock function.

Note that the Security Erase Unit command initializes from LBA 0 to Native MAX LBA. Host MAX LBA set by Initialize Drive Parameter, and Device Configuration Overlay is ignored. So the protected area is also initialized.

This command requests to transfer a single sector data from the host including information specified in Table 202 on the page 246.

When security is disabled and the Identifier bit is set to User, then the device shall return command aborted.

If the password does not match, then the device rejects the command with an Aborted error.

The Security Erase Unit command erases all user data and disables the security mode feature (device lock function). So after completing this command, all user data will be initialized to zero with write operation. At this time, it is not verified with read operation whether the sector of data is initialized correctly. Also, the defective sector information and the reassigned sector information for the device are not updated. The security erase prepare

command should be completed immediately prior to the Security Erase Unit command. If the device receives a Security Erase Unit command without a prior Security Erase Prepare command, the device aborts the security erase unit command.

This command disables the security mode feature (device lock function), however the master password is still stored internally within the device and may be re-activated later when a new user password is set. If you execute this command on disabling the security mode feature (device lock function), the password sent by the host is NOT compared with the password stored in the device for both the Master Password and the User Password, and then the device only erases all user data.

The execution time of this command is set in word 89 of Identify device information.

Table 163 Security Erase Unit Command (F4h)

Command Block Output Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	1	0	1	0	0

Command Block Input Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below…							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Table 164   Erase Unit Information

Word	Description
00	Control word bit 0 : Identifier (1-Mater, 0-User) bit 1 : Erase mode (1- Enhanced, 0- Normal) Enhanced mode is not supported bit 2-15 : Reserved
01-16	Password (32 bytes)
17-255	Reserved

Identifier   Zero indicates that the device should check the supplied password against the user password stored internally. One indicates that the device should check the given password against the master password stored internally.

Normal Outputs

See Normal Outputs in Section 11.5 Flush Cache (E7h)

Error Outputs

See Error Outputs in Section 11.2 Download Microcode (92h)

The device shall return command aborted if:

    a)   this command was not immediately preceded by a SECURITY ERASE PREPARE command;
    b)   the ERASE MODE bit was set to one and the device does not support Enhanced Erase mode;
    c)   the contents of the PASSWORD field do not match the stored password;
    d)   the PASSWORD field contained an invalid value; or
    e)   the data area is not successfully overwritten.

device may return command completion with the ERROR bit set to one if an Interface CRC error has occurred.

11.32 Security Freeze Lock (F5h)

The Security Freeze Lock Command allows the device to enter frozen mode immediately.

After this command is completed, the command which updates Security Mode Feature (Device Lock Function) is rejected.

Frozen mode is quit only by Power off.

The following commands are rejected when the device is in frozen mode. For detail, refer to Table 33 and Table 34 on the page 62-63.

- Security Set Password
- Security Unlock
- Security Disable Password
- Security Erase Unit

Table 165 Security Freeze Lock Command (F5h)

Command Block Output Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	1	0	1	0	1

Command Block Input Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below…							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

11.33 Security Set Password (F1h)

The Security Set Password command enables security mode feature (device lock function), and sets the master password or the user password.

The security mode feature (device lock function) is enabled by this command, and the device is not locked immediately. The device is locked after next power on reset. When the MASTER password is set by this command, the master password is registered internally, but the device is NOT locked after next power on reset or hard reset.

This command requests a transfer of a single sector of data from the host including the information specified in the following Table.

Table 166   Security Set Password Command (F1h)

Command Block Output Registers										Command Block Input Registers								
Register	7	6	5	4	3	2	1	0		Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-		Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-		Error			…See Below…					
Sector Count	-	-	-	-	-	-	-	-		Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-		Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-		Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-		Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-		Device/Head	-	-	-	-	-	-	-	-
Command	1	1	1	1	0	0	0	1		Status			…See Below…					

	Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

	Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

The data transferred controls the function of this command.

Table 167   Security Set Password Information

Word	Description	
00	Control word	
	bits 15:9	Reserved
	bit 8	Security level (1-Maximum, 0-High)
	bits 7:1	Reserved
	bit 0	Identifier (1-Master, 0-User)
01-16	Password (32 byte)	
17	Master Password Identifier Code (valid if Word 0 bit 0 = 1)	
18-255	Reserved	

Identifier   Zero indicates that the device regards Password as User Password. One indicates that device regards Password as Master Password.

Security Level   Zero indicates High level, one indicates Maximum level. If the host sets High level and the password is forgotten, then the Master Password can be used to unlock the device. If the host sets Maximum level and the user password is forgotten, only a Security Erase Prepare/Security Unit command can unlock the device and all data will be lost.

Password   The text of the password – all 32 bytes are always significant.

Master Password   The revision code field is returned in the IDENTIFY DEVICE word 92.
Revision Code   The valid revision codes are 0001h through FFFEh. The device accepts the command with a value of 0000h or FFFFh in this field, but does not change Master Password Revision code.

The setting of the Identifier and Security level bits interact as follows.

Identifier=User / Security level = High
The password supplied with the command will be saved as the new user password. The security mode feature (lock function) will be enabled from the next power on. The file may then be unlocked by either the user password or the previously set master password.

Identifier=Master / Security level = High
This combination will set a master password but will NOT enable the security mode feature (lock function).

Identifier=User / Security level = Maximum
The password supplied with the command will be saved as the new user password. The security mode feature (lock function) will be enabled from the next power on. The file may then be unlocked by only the user password. The master password previously set is still stored in the file but may NOT be used to unlock the device.

Identifier=Master / Security level = Maximum
This combination will set a master password but will NOT enable the security mode feature (lock function).

11.34 Security Unlock (F2h)

This command unlocks the password and causes the device to enter device unlock mode. If power on reset or hard reset is done without executing the Security Disable Password command after this command is completed, the device will be in device lock mode. The password has not been changed yet.

The Security Unlock command requests to transfer a single sector of data from the host including information specified in the following Tables.

Table 168   Security Unlock Command (F2h

Command Block Output Registers	7	6	5	4	3	2	1	0		Command Block Input Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0		Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-		Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-		Error				…See Below…				
Sector Count	-	-	-	-	-	-	-	-		Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-		Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-		Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-		Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-		Device/Head	-	-	-	-	-	-	-	-
Command	1	1	1	1	0	0	1	0		Status				…See Below…				

Error Register								Status Register							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN	BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	0	0	V	0	0	0	V	0	-	-	0	-	V

If the Identifier bit is set to master and the file is in high security mode then the password supplied will be compared with the stored master password. If the file is in maximum security mode the security unlock will be rejected.

If the Identifier bit is set to user, then the file compares the supplied password with the stored user password.

If the password compare fails, then the device returns an abort error to the host and decrements the unlock attempt counter. This counter is initially set to 5 and is decremented for each password mismatch.

When security is disabled and the Identifier bit is set to User, then the device shall return command aborted.

When this counter reaches zero then all password protected commands are rejected until a hard reset or a power off.

Table 169 Security Unlock Information

Word	Description

00	Control word
	    bit 0 : Identifier (1-Mater, 0-User)
	    bit 1-15 : Reserved

01-16	Password (32 bytes)
17-255	Reserved

Identifier   Zero indicates that device regards Password as User Password. One indicates that device regards Password as Master Password.

The user can detect if the attempt to unlock the device has failed due to a mismatched password as this is the only reason that an abort error will be returned by the file AFTER the password information has been sent to the device. If an abort error is returned by the device BEFORE the password data has been sent to the file then another problem exists.

Normal Outputs

See Normal Outputs in Section 11.5 Flush Cache (E7h)

Error Outputs

See Error Outputs in Section 11.2 Download Microcode (92h)

11.35 Seek (7xh)

The Seek command initiates a seek to the designated track and selects the designated head. The device need not be formatted for a seek to execute properly.

Table 170   Seek Command (7xh)

Command Block Output Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	1	L	1	D	H	H	H	H
Command	0	1	1	1	-	-	-	-

Command Block Input Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below…							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	-	-	-	-	H	H	H	H
Status	…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Output Parameters To The Device

Sector Number	In LBA mode, this register specifies LBA address bits 0 – 7 for seek. (L=1)
Cylinder High/Low	The cylinder number of the seek. In LBA mode, this register specifies LBA address bits 8 – 15 (Low), 16 – 23 (High) for seek. (L=1)
H	The head number of the seek. In LBA mode, this register specifies LBA address bits 24 – 27 for seek. (L=1)

Input Parameters From The Device

Sector Number	In LBA mode, this register contains current LBA bits 0 – 7. (L=1)
Cylinder High/Low	In LBA mode, this register contains current LBA bits 8 – 15 (Low), 16 – 23 (High). (L=1)
H	In LBA mode, this register contains current LBA bits 24 – 27. (L=1)

11.36   Set Features (EFh)

The Set Feature command is to establish the following parameters which affect the execution of certain features as shown in below table.

ABT will be set to 1 in the Error Register if the Feature register contains any undefined values.

Table 171   Set Features Command (EFh)

Command Block Output Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	V	V	V	V	V	V	V	V
Sector Count				Note.1				
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	0	1	1	1	1

Command Block Input Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error				…See Below…				
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status				…See Below…				

Error Register								
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register								
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

Output Parameters To The Device

Feature   Destination code for this command

02H	Enable write cache
03H	Set transfer mode based on value in sector count register
05H	Enable Advanced Power Management
06H	Enable Power-up in Standby feature set
07H	Power-Up In Standby feature set device spin-up
10H	Enable use of Serial ATA feature
4Ah	Extended Power Conditions
55H	Disable read look-ahead feature
63h	Enable/Disable the DSN feature set
66H	Disable reverting to power on defaults
82H	Disable write cache
85H	Disable Advanced Power Management
86H	Disable Power-up in Standby mode
90H	Disable use of Serial ATA feature
AAH	Enable read look-ahead feature
CCH	Enable reverting to power on defaults
C3h	Enable/Disable the Sense Data Reporting feature set
C4h	Enable/Disable sense data return for successful NCQ commands

Note.

After power on reset or hard reset, the device is set to the following features as default.

Write cache   : Enable

Read look-ahead   : Enable
Reverting to power on defaults   : Disable
Release interrupt   : Disable

11.36.1 Set Transfer Mode

When Feature register is 03h (=Set Transfer Mode), the Sector Count Register specifies the transfer mechanism. The upper 5 bits define the type of transfer and the low order 3 bits encode the mode value.

PIO Default Transfer Mode	00000	000	
PIO Default Transfer Mode	00000	001	
Disable IORDY			
PIO Flow Control Transfer Mode x	00001	nnn	(nnn=000,001,010,011,100)
Multiword DMA mode x	00100	nnn	(nnn=000,001,010)
Ultra DMA mode x	01000	nnn	(nnn=000,001,010,011,100,101,110)

11.36.2 Write Cache

If the number of auto reassigned sector reaches the device's reassignment capacity, the write cache function will be automatically disabled. Although the device still accepts the Set Features command with Feature register = 02h without error, but the write cache function will remains disabled. For current write cache function status, please refer to Identify Device Information (word 85 or 129) by Identify Device command.

11.36.3 Serial ATA Feature

When the Feature register is set to 10h or 90h, the value set to the Sector Count register specifies the specific Serial ATA feature to enable or disable.

Sector Count Value	Description
02h	DMA Setup FIS Auto-Activate optimization
03h	Device-initiated interface power state transitions
06h	Software Settings Preservation

11.36.4 Advanced Power Management

When the value in the Feature register is 05h (=Enable Advanced Power Management), the Sector Count Register specifies the Advanced Power Management level.

FFh ---	Aborted
C0 – FEh ---	The deepest power saving mode is Idle mode (the same as Disable Advanced Power Management)
80 – BFh ---	The deepest power saving mode is Low power Idle mode
01 – 7Fh ---	The deepest power saving mode is Low RPM Idle mode
00h ---	Aborted

The idle time to Low power idle mode and Low RPM idle mode vary according to the value in Sector Count Register as follows:

When Low power idle mode is the deepest power saving mode,

$Y_1=(x-80h) * 5+120$ [sec]   ($120<= Y_1<=435$)

Y_2=N/A(the device does not go to Low RPM idle mode)

When Low RPM idle mode is the deepest power saving mode and the value in Sector Count Register is between 40h and 7Fh,

$120<= Y_1<=435$ [sec]   (default: 120 [sec])

$Y_2=(x-40h) * 60 + 600$[sec]   ($600<= Y_2<=4380$)

When Low RPM idle mode is the deepest power saving mode and the value in Sector Count Register is between 01h and 3Fh,

$120<= Y_1<=435$ [sec]   (default: 120 [sec])

$Y_2=600$ [sec]

Where x is the value in Sector Count Register, y_1 is the idle time to Low Power Idle mode, and y_2 is the idle time to Low RPM idle mode.

If Low power idle mode has already been enabled (i.e., y_1 has been set) before Low RPM idle mode is enabled, y_1 is preserved. If Low power idle mode is disabled (i.e., y_1 has not been set yet), y_1 becomes 120[sec] when Low RPM idle mode is enabled.

Enabled power saving mode and idle time (y_1 and y_2) are preserved until Advanced Power Management is disabled, the deepest power saving mode becomes Idle mode, or new time is set. They are initialized with a hard/soft reset unless Reverting to power on defaults is disabled and the device receives a soft reset.

11.36.5   Extended Power Conditions (EPC) Feature

11.36.5.1   Restore Power Condition Settings subcommand

Table 172   Restore Power Condition Settings subcommand

Command Block Output Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	0	1	0	0	1	0	1	0
Sector Count	V	V	V	V	V	V	V	V
Sector Number	-	V	-	V	0	0	0	0
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	0	1	1	1	1

Command Block Input Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below…							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

On successful completion of this EPC subcommand, the device updates the Power Conditions log for the selected Power Condition ID as follows:

1) if Default is set to one, then:
   A) copy the Default Timer Settings field to the Current Timer Settings field; and
   B) copy the Default Timer Enabled field to the Current Timer Enabled field;
2) if Default is cleared to zero, then:
   A) copy the Saved Timer Settings field to the Current Timer Settings field; and
   B) copy the Saved Timer Enabled field to the Current Timer Enabled field;
   and
3) if Save is set to one and the power condition is savable, then:
   A) copy the Current Timer Settings field to the Saved Timer Settings field;

Output Parameters To The Device

Sector Count   Power Condition ID (*See Table 69, Section 9.20*)

Sector Number	**bit**	**Description**
	7	Reserved
	6	Default
		1 Restore from Default settings
		0 Restore from Saved settings
	5	Reserved
	4	Save
		1 Save settings on completion
		0 Do not save settings on completion
	3-0	0h Restore Power Condition subcommand (See Table 70)

Error Output
If any selected Power Condition is not supported, or is not changeable, or if Extended Power Condition feature set is disable, or if Save is set to one and any selected power condition is not savable, then the device returns command aborted.

11.36.5.2   Go To Power Condition Subcommand

Table 173   Go To Power Condition subcommand

Command Block Output Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	0	1	0	0	1	0	1	0
Sector Count	V	V	V	V	V	V	V	V
Sector Number	-	-	-	-	0	0	0	1
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	0	1	1	1	1

Command Block Input Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below…							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

On successful completion of this EPC subcommand, the device:

1) stops all enabled EPC timers;

2) enters the selected EPC power condition after command completion of the SET FEATURES command without having to wait for any timers to expire; and

3) the device remains in the selected power condition until the device processes the next command or reset.

Output Parameters To The Device

Sector Count   Power Condition ID (*See Table 69, Section 9.20*)

Sector Number	**bit**	**Description**
	7-4	Reserved
	3-0	1h Go To Power Condition subcommand (See Table 70)
Device/Head	**1**	DELAYED ENTRY bit
	0	HOLD POWER CONDITION bit

Error Output

If the Power Condition ID is FFh, a reserved value, or is not supported, or if Extended Power Condition feature set is disable, then the device returns command aborted .

11.36.5.3   Set Power Condition Timer Subcommand

Table 174   Set Power Condition Timer subcommand

Command Block Output Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	0	1	0	0	1	0	1	0
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	-	V	V	0	0	1	0
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	0	1	1	1	1

Command Block Input Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below…							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

On successful completion of this EPC subcommand, the device updates the Power Conditions log for the selected and supported Power Condition as follows:

1) copy the Timer field to the Current Timer Settings field;

2) if Enable is set to one and the Timer field is non-zero, then enable the Current Timer;

3) if Enable is set to one and the Timer field is zero, then disable the Current Timer;

4) if Enable is cleared to zero, then disable the Current Timer; and

5) if Save is set to one and the Power Condition settings are savable, then:

   A) copy the Current Timer Settings field to the Saved Timer Settings field; and

   B) copy the Current Timer Enabled field to the Saved Timer Enabled field.

Output Parameters To The Device

Sector Count   Power Condition ID (*See Table 69, Section 9.20*)

Sector Number	**bit**	**Description**
	7	Timer Units
		If the Timer Units bit is cleared to zero, then the Timer (Cylinder High and Cylinder Low bit 15-0) are specified in units of 100 milliseconds. If the Timer Units bit is set to one, then the Timer (Cylinder High and Cylinder Low bit 15-0) are specified in units of 1 minute.
	6	Reserved
	5	Enable
	1	Enable the selected power condition
	0	Disable the selected power condition
	4	Save
	1	Save settings on completion
	0	Do not save settings on completion
	3-0	2h Set Power Condition Timer subcommand (See Table 70)

Cylinder Low **Cylinder High**	**15-0**	If the new timer value is greater than the maximum value setting, then the device set the value to the maximum setting. If the new timer value is less than the minimum setting, then the device set the value to the minimum setting.
		(Cylinder High and Cylinder Low bit 15-0)

Error Output

The device returns command aborted If:

a) the new timer value is:
- A) less than the maximum setting.
- B) greater than the minimum setting.
- C) not supported by the device.

b) the Extended Power Condition feature set is disabling.

c) the power condition is not changeable or not supported.

d) the Save bit is set to one and the selected power condition is not savable.

e) the new time value is greater than the maximum setting and the device did not set the timer to the maximum setting.

f) the new time value is less than the minimum setting and the device did not set the timer to the minimum setting.

If command aborted is returned, then the device makes no modifications to the power condition settings.

Maximum Setting is 3BFFC4h (100ms unit). Minimum Setting is zero.

11.36.5.4 Set Power Condition State Subcommand

Table 175 Set Power Condition State subcommand

Command Block Output Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	0	1	0	0	1	0	1	0
Sector Count	V	V	V	V	V	V	V	V
Sector Number	-	-	V	V	0	0	1	1
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	0	1	1	1	1

Command Block Input Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below…							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

On successful completion of this EPC subcommand, the device updates the Power Conditions log for the Power Condition as follows:

1) If the Enable bit is set to one, then enable the Current Timer; otherwise disable the Current Timer; and

2) If the Save bit is set to one, then copy the Current Timer Enabled field to the Saved Timer Enabled field.

Output Parameters To The Device

Sector Count Power Condition ID (*See Table 69, Section 9.20 *)

Sector Number **bit Description**

7-6 Reserved

5 Enable

   1 Enable the selected power condition

   0 Disable the selected power condition

4 Save

   1 Save settings on completion

   0 Do not save settings on completion

3-0 3h Set Power Condition State subcommand (See Table 70)

Error Output

If the Power Condition is not changeable, or not supported, or if Extended Power Conditions feature set is disabling, then the device returns command aborted. If the Save bit is set to one and the selected power condition is not savable, then the device returns command aborted. If command aborted is returned, then the device makes no modifications to the power condition settings.

11.36.5.5   Enable the EPC Feature Subcommand

Table 176   Enable the EPC feature subcommand

Command Block Output Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	0	1	0	0	1	0	1	0
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	0	1	0	0
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	0	1	1	1	1

Command Block Input Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below…							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

On successful completion of this EPC subcommand, the device:

a) enables the EPC feature set;

b) sets IDENITFY DEVICE data word 120 bit 7 to one; and

c) disables the APM feature set.

d) if the Saved Timer Setting field is cleared to zero, then:
copy the value of the Default Timer Setting to the Current Timer Setting; and

e) if the Saved Timer Setting field is non-zero, then:
copy the value of the Saved Timer Setting to the Current Timer Setting; and

f) if the Current Timer Setting field is non-zero and the Current Timer Enabled is set to one,
then initialize and start the timer.

If the EPC feature set is enabled, then the EPC feature set remains enabled across all resets (i.e., power-on reset, hardware reset, and software reset).

Output Parameters To The Device

Sector Number   bit Description

　　　　　　　　　　7-4 Reserved

　　　　　　　　　　3-0 4h Enable the EPC feature subcommand (*See Table 178 above*)

Error Output

If the Extended Power Condition feature set is not supported then the device returns command aborted.

11.36.5.6   Disable the EPC Feature Subcommand

Table 177   Disable the EPC feature subcommand

Command Block Output Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	0	1	0	0	1	0	1	0
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	0	1	0	1
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	0	1	1	1	1

Command Block Input Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below…							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

On successful completion of this EPC subcommand, the device:

  a) stop all EPC timers
  b) disables the EPC feature set; and
  c) clears IDENITFY DEVICE data word 120 bit 7 to zero.

If the EPC feature set is disabled, then the EPC feature set remains disabled across all resets (i.e., power-on reset, hardware reset, and software reset).

Output Parameters To The Device

Sector Number　　**bit**　**Description**

　　　　　　　　　7-4　Reserved
　　　　　　　　　3-0　5h Disable the EPC feature subcommand (*See Table 178 in* <u>*Section 11.37.5.5*</u> *)*

Error Output

If the Extended Power Condition feature set is disabling, not supported then the device returns command aborted.

11.37   Set Multiple (C6h)

The Set Multiple command enables the device to perform Read and Write Multiple commands and establishes the block size for these commands. The block size is the number of sectors to be transferred for each interrupt.

If an invalid block size is specified, an Abort error will be returned to the host, and Read Multiple and Write Multiple commands will be disabled.

Table 178   Set Multiple Commands (C6h)

Command Block Output Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	0	0	0	1	1	0

Command Block Input Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below…							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

Output Parameters To The Device

Sector Count.   The block size to be used for Read Multiple and Write Multiple commands. Valid block sizes can be selected from 0, 1, 2, 4, 8 or 16. If 0 is specified, then Read Multiple and Write Multiple commands are disabled.

11.38 Sleep (E6h/99h)

This command causes the device to enter Sleep Mode.

The device is spun down and the interface becomes inactive. If the device is already spun down, the spin down sequence is not executed.

The only way to recover from Sleep Mode is with software reset or hardware reset.

Table 179 Sleep Command (E6h/99h)

Command Block Output Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	0	0	1	1	0

Command Block Input Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below…							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	…See Below…							

			Error Register				
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

			Status Register				
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

11.39   SMART Function Set (B0h)

The SMART Function Set command provides access to Attribute Values, Attribute Thresholds and other low level subcommands that can be used for logging and reporting purposes and to accommodate special user needs. The SMART Function Set command has several separate subcommands which are selectable via the device's Features Register when the SMART Function Set command is issued by the host.

Table 180   SMART Function Set Command (B0h)

Command Block Output Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	V	V	V	V	V	V	V	V
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	0	1	0	0	1	1	1	1
Cylinder High	1	1	0	0	0	0	1	0
Device/Head	1	-	1	D	-	-	-	-
Command	1	0	1	1	0	0	0	0

Command Block Input Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below…							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	V	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

11.39.1   SMART Subcommand

In order to select a subcommand the host must write the subcommand code to the device's Features Register before issuing the SMART Function Set command. The subcommands and their respective codes are listed below.

Code	Subcommand
D0h	SMART Read Attribute Values
D1h	SMART Read Attribute Thresholds
D2h	SMART Enable/Disable Attribute Autosave
D3h	SMART Save Attribute Values
D4h	SMART Execute Off-line Immediate
D5h	SMART Read Log Sector
D6h	SMART Write Log Sector
D8h	SMART Enable Operations
D9h	SMART Disable Operations
DAh	SMART Return Status
DBh	SMART Enable/Disable Automatic Off-Line

11.39.1.1   SMART Read Attribute Values (Subcommand D0h)

This subcommand returns the device's Attribute Values to the host. Upon receipt of the SMART Read Attribute Values subcommand from the host, the device transfers 512 bytes of Attribute Value information to the host.

11.39.1.2   SMART Read Attribute Thresholds (Subcommand D1h)

This subcommand returns the device's Attribute Thresholds to the host. Upon receipt of the SMART Read Attribute Thresholds subcommand from the host, the transfers 512 bytes of Attribute Thresholds information to the host.

11.39.1.3   SMART Enable/Disable Attribute Autosave (Subcommand D2h)

This subcommand Enables and Disables the Attribute Autosave feature of the device. The SMART Enable/Disable Attribute Autosave subcommand either allows the device to automatically save its updated Attribute Values to the Attribute Data Sector periodically; or this subcommand causes the Autosave feature to be disabled. The state of the Attribute Autosave feature (either enabled or disabled) will be preserved by the device across power cycle.

A value of 00h written by the host into the device's Sector Count Register before issuing the SMART Enable/Disable Attribute Autosave subcommand will cause this feature to be disabled. Disabling this feature does not preclude the device from saving Attribute Values to the Attribute Data sectors during some other normal operation such as during a power-up or power-down.

A value of F1h written by the host into the device's Sector Count Register before issuing the SMART Enable/Disable Attribute Autosave subcommand will cause this feature to be enabled. Any other non-zero value written by the host into this register before issuing the SMART Enable/Disable Attribute Autosave subcommand will not change the current Autosave status but the device will respond with the error code specified in Table 242.

The SMART Disable Operations subcommand disables the Autosave feature along with the device's SMART operations.

Upon the receipt of the subcommand from the host, the device asserts BSY, Enables or Disables the Autosave feature, clears BSY and asserts INTRQ.

Command Input

Field	Description	
FEATURE	D2h	
COUNT	Value	Description
	00h	Disable attribute autosave

	01h-F0h N/A
	F1h Enable attribute autosave
	F2h-FFh N/A
LBA	**Bit Description**
	27:24 N/A
	23:8 C24Fh
	7:0 N/A
DEVICE	**Bit Description**
	7 Obsolete
	6 N/A
	5 Obsolete
	4 Transport Dependent
	3:0 Reserved
Command	7:0 B0h

Normal Outputs

See Normal Outputs in *Section 11.5 "Flush Cache (E7h)"*

Error Outputs

See Error Outputs in *Section 11.8 "Idle (E3h/97h)"*

11.39.1.4   SMART Save Attribute Values (Subcommand D3h)

This subcommand causes the device to immediately save any updated Attribute Values to the device's Attribute Data sector regardless of the state of the Attribute Autosave feature. Upon receipt of the SMART Save Attribute Values subcommand from the host, the device writes any updated Attribute Values to the Attribute Data sector.

11.39.1.5   SMART Execute Off-line Immediate (Subcommand D4h)

This subcommand causes the device to immediately initiate the set of activities that collect Attribute data in an off-line mode (off-line routine) or execute a self-test routine in either captive or off-line mode.

The Sector Number register shall be set to specify the operation to be executed.

Sector Number	Operation to be executed
0	Execute SMART off-line data collection routine immediately
1	Execute SMART Short self-test routine immediately in off-line mode
2	Execute SMART Extended self-test routine immediately in off-line mode
4	Execute SMART Selective self-test routine immediately in off-line mode
127	Abort off-line mode self-test routine
129	Execute SMART Short self-test routine immediately in captive mode
130	Execute SMART Extended self-test routine immediately in captive mode
132	Execute SMART Selective self-test routine immediately in captive mode

Off-line mode: The device executes command completion before executing the specified routine. During execution of the routine the device will not set BSY nor clear DRDY. If the device is in the process of performing its routine and is interrupted by a new command from the host, the device will abort or suspend its routine and service the host within two seconds after receipt of the new command. After servicing the interrupting command, the device will resume its routine automatically or not start its routine depending on the interrupting command.

Captive mode: When executing self-test in captive mode, the device sets BSY to one and executes the specified self-test routine after receipt of the command. At the end of the routine, the device sets the execution result in the Self-test execution status byte (*Table 187 "Device Attribute Data Structure"*) and ATA registers as below and executes command completion.

Status   Set ERR to one when self-test has failed

Error   Set ABRT to one when self-test has failed

Cyl Low   Set to F4h when self-test has failed

Cyl High   Set to 2Ch when self-test has failed

11.39.1.6   SMART Read Log Sector (Subcommand D5h)

This command returns the specified log sector contents to the host.

The 512 bytes data are returned at a command and the Sector Count value shall be set to one. The Sector Number shall be set to specify the log sector address.

Table 181   Log sector addresses

Log sector address	Content	Type
00h	Log directory	Read Only
01h	Summary SMART Error Log	Read Only
03h	Extended Comprehensive SMART Error Log	See Note
06h	SMART Self-test Log	Read Only
07h	Extended Self-test Log	See Note
09h	Selective self-test Log	Read/Write
80h-9Fh	Host vendor specific	Read/Write

Note: Log addresses 03h and 07h are used by the Read Log Ext and Write Log Ext commands. If these log addresses are used with the SMART Read Log Sector command, the device shall return command aborted.

11.39.1.7   SMART Write Log Sector (Subcommand D6h)

This command writes 512 bytes data to the specified log sector.

The 512 bytes data are transferred at a command and the Sector Count value shall be set to one. The Sector Number shall be set to specify the log sector address (*Table 186 above*). If Read Only log sector is specified, the device returns ABRT error.

11.39.1.8   SMART Enable Operations (Subcommand D8h)

This subcommand enables access to all SMART capabilities within the device. Prior to receipt of a SMART Enable Operations subcommand, Attribute Values are neither monitored nor saved by the device. The state of SMART (either enabled or disabled) will be preserved by the device across power cycles. Once enabled, the receipt of subsequent SMART Enable Operations subcommands will not affect any of the Attribute Values.

Upon receipt of the SMART Enable Operations subcommand from the host, the device enables SMART capabilities and functions, and then saves any updated Attribute Values to the Attribute Data sector.

11.39.1.9   SMART Disable Operations (Subcommand D9h)

This subcommand disables all SMART capabilities within the device including the device's attribute autosave feature. After receipt of this subcommand the device disables all SMART operations. Non self-preserved Attribute Values will no longer be monitored. The state of SMART (either enabled or disabled) is preserved by the device across power cycles.

Upon receipt of the SMART Disable Operations subcommand from the host, the device disables SMART capabilities and functions, and then saves any updated Attribute Values to the Attribute Data sector.

After receipt of the device of the SMART Disable Operations subcommand from the host, all other SMART subcommands – with the exception of SMART Enable Operations – are disabled, and invalid and will be aborted by the device (including the SMART Disable Operations subcommand), returning the error code as specified in Table 242 on the page 290.

Any Attribute Values accumulated and saved to volatile memory prior to receipt of the SMART Disable Operations command will be preserved in the device's Attribute Data Sectors. If the device is re-enabled, these Attribute Values will be updated, as needed, upon receipt of a SMART Read Attribute Values or SMART Save Attribute Values command.

11.39.1.10   SMART Return Status (Subcommand DAh)

This command is used to communicate the reliability status of the device to the host's request. Upon receipt of the SMART Return Status subcommand the device saves any updated Pre-failure type Attribute Values to the reserved sector and compares the updated Attribute Values to the Attribute Thresholds.

If the device does not detect a Threshold Exceeded Condition, the device loads 4Fh into the Cylinder Low register, C2h into the Cylinder High register.

If the device detects a Threshold Exceeded Condition, the device loads F4h into the Cylinder Low register, 2Ch into the Cylinder High register.

11.39.1.11   SMART Enable/Disable Automatic Off-Line (Subcommand DBh)

This subcommand enables and disables the optional feature that causes the device to perform the set of off-line data collection activities that automatically collect attribute data in an off-line mode and then save this data to the device's non-volatile memory. This subcommand may either cause the device to automatically initiate or resume performance of its off-line data collection activities or cause the automatic off-line data collection feature to be disabled.

A value of zero written by the host into the device's Sector Count Register before issuing this subcommand shall cause the feature to be disabled. Disabling this feature does not preclude the device from saving attribute values to non-volatile memory during some other normal operation such as during a power-on or power-off sequence or during an error recovery sequence.

A value of F8h written by the host into the device's Sector Count Register before issuing this subcommand shall cause this feature to be enabled. Any other non-zero value written by the host into this register before issuing this subcommand is vender specific and will not change the current Automatic Off-Line Data Collection, but the device may respond with the error code specified in Table 199 "*SMART Error Codes*" in *Section 11.40.8*).

11.39.2   Device Attributes Data Structure

The following Table defines the 512 bytes that make up the Attribute Value information. This data structure is accessed by the host in its entirety using the SMART Read Attribute Values subcommand. All multi-byte fields shown in these data structures are in byte ordering, namely that the least significant byte occupies the lowest numbered byte address location in the field.

Table 182   Device Attribute Data Structure

Description	Bytes	Offset	Value
Data Structure Revision Number	2	00h	0010h
1st Device Attribute	12	02h	
…	..		
…	..		
30th Device Attribute	12	15Eh	
Off-line data collection status	1	16Ah	
Self-test execution status	1	16Bh	
Total time in seconds to complete off-line data collection activity	2	16Ch	
Vender specific	1	16Eh	
Off-line data collection capability	1	16Fh	1Bh
SMART capability	2	170h	0003h
SMART device error logging capability	1	172h	01h
Self-test failure check point	1	173h	
Short self-test completion time in minutes	1	174h	
Extended self-test completion time in minutes. If 0FFh, use bytes 177h and 178h for completion time.	1	175h	
Reserved	1	176h	
Extended self-test completion time in minutes. (word)	2	177h	
Reserved	9	179h	
Vendor specific	125	182h	
Data structure checksum	1	1FFh	
	512		

11.39.2.1   Data Structure Revision Number

The Data Structure Revision Number identifies which version of this data structure is implemented by the device. This revision number identifies both the Attribute Value and Attribute Threshold Data structures.

11.39.2.2   Individual Attribute Data Structure

The following Table defines the 12 bytes that make up the information for each Attribute entry in the Device Attribute Data Structure.

Table 183   Individual Attribute Data Structure

Description	Bytes	Offset
Attribute ID Number (01h to FFh)	1	00h
Status Flags	2	01h
Attribute Value (valid values from 01h to FDh)	1	03h
Vender specific	8	04h
Total Bytes	12	

Attribute ID Numbers: Any non-zero value in the Attribute ID Number indicates an active attribute. The device supports following Attribute ID Numbers.

ID	Attribute Name
0	Indicates that this entry in the data structure is not used
1	Raw Read Error Rate
2	Throughput Performance
3	Spin Up Time
4	Start/Stop Count
5	Reallocated Sector Count
7	Seek Error Rate
8	Seek Time Performance
9	Power-On Hours Count
10	Spin Retry Count
11	Drive Calibration Retry Count
12	Device Power Cycle Count
192	Power off Retract count
193	Load Cycle count
194	Temperature
196	Reallocation Event Count
197	Current Pending Sector Count
198	Off-Line Scan Uncorrectable Sector Count
199	Ultra DMA CRC Error Count
241	Total LBAs Written
242	Total LBAs Read

Status Flag Definitions

Bit	Definition
0	Pre-failure/advisory bit

	0	An Attribute Value less than or equal to its corresponding Attribute Threshold indicates an advisory condition where the usage or age of the device has exceeded its intended design life period.
	1	An Attribute Value less than or equal to its corresponding attribute threshold indicates a pre-Failure condition where imminent loss of data is being predicted.

1	On-Line Collective bit

	0	The Attribute Value is updated only during Off-Line testing
	1	The Attribute Value is updated during On-Line testing or during both On-Line and Off-Line testing.

2-5	Vendor specific
6-15	Reserved (0)

Normalized Values: The device will perform conversion of the raw Attribute Values to transform them into normalized values, which the host can then compare with the Threshold values. A Threshold is the excursion limit for a normalized Attribute Value.

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11.39.2.3   Off-Line Data Collection Status

The value of this byte defines the current status of the off-line activities of the device. Bit 7 indicates Automatic Off-Line Data Collection Status.

Bit 7   Automatic Off-Line Data Collection Status

0   Automatic Off-Line Data Collection is disabled.

1   Automatic Off-Line Data Collection is enabled.

Bits 0 thru 6 represent a hexadecimal status value reported by the device.

Value   Definition

0   Off-line data collection never started

2   All segments completed without errors.

4   Off-line data collection suspended by interrupting command

5   Off-line data collecting aborted by interrupting command

6   Off-line data collection aborted with fatal error

11.39.2.4   Self-Test Execution Status

Bit   Definition

0-3   Percent Self-test remaining

An approximation of the percent of the self-test routine remaining until completion in ten percent increments. Valid values are 0 through 9.

4-7   Current Self-test execution status

0   The self-test routine completed without error or has never been run

1   The self-test routine aborted by the host

2   The self-test routine interrupted by the host with a hard or soft reset

3   The device was unable to complete the self-test routine due to a fatal error or unknown test error

4   The self-test routine completed with unknown element failure

5   The self-test routine completed with electrical element failure

6   The self-test routine completed with servo element failure

7   The self-test routine completed with read element failure

15   The self-test routine in progress

11.39.2.5   Total Time in Seconds to Complete Off-line Data Collection Activity

This field tells the host how many seconds the device requires completing the off-line data collection activity.

11.39.2.6   Off-Line Data Collection Capability

Bit   **Definition**

0   Execute Off-line Immediate implemented bit

    0   SMART Execute Off-line Immediate subcommand is not implemented

    1   SMART Execute Off-line Immediate subcommand is implemented

1   Enable/disable Automatic Off-line implemented bit

    0   SMART Enable/disable Automatic Off-line subcommand is not implemented

    1   SMART Enable/disable Automatic Off-line subcommand is implemented

2   abort/restart off-line by host bit

    0   The device will suspend off-line data collection activity after an interrupting command and resume it after some vendor specific event

    1   The device will abort off-line data collection activity upon receipt of a new command

3   Off-line Read Scanning implemented bit

    0   The device does not support Off-line Read Scanning

    1   The device supports Off-line Read Scanning

4   Self-test implemented bit

    0   Self-test routine is not implemented

    1   Self-test routine is implemented

5-7   Reserved (0)

6   Selective self-test implemented bit

    0   Selective self-test routine is not implemented

    1   Selective self-test routine is implemented

11.39.2.7   SMART Capability

This word of bit flags describes the SMART capabilities of the device. The device will return 03h indicating that the device will save its Attribute Values prior to going into a power saving mode and supports the SMART ENABLE/DISABLE ATTRIBUTE AUTOSAVE command.

Bit   **Definition**

0   Pre-power mode attribute saving capability
    If bit = 1, the device will save its Attribute Values prior to going into a power saving mode (Standby or Sleep mode).

1   Attribute autosave capability
    If bit = 1, the device supports the SMART ENABLE/DISABLE ATTRIBUTE AUTOSAVE command.

2-15   Reserved (0)

11.39.2.8   Error Logging Capability

Bit   **Definition**

7-1   Reserved (0)

0   Error Logging support bit
    If bit = 1, the device supports the Error Logging

11.9.2.8   Self-Test Failure Check Point

This byte indicates the section of self-test where the device detected a failure.

11.39.2.10   Self-Test Completion Time

These bytes are the minimum time in minutes to complete self-test.

11.39.2.11   Data Structure Checksum

The Data Structure Checksum is the 2's compliment of the result of a simple 8-bit addition of the first 511 bytes in the data structure.

11.39.3   Device Attribute Thresholds Data Structure

The following Table defines the 512 bytes that make up the Attribute Threshold information. This data structure is accessed by the host in its entirety using the SMART Read Attribute Thresholds. All multi-byte fields shown in these data structures follow the ATA/ATAPI-7 specification for byte ordering, namely that the least significant byte occupies the lowest numbered byte address location in the field.

The sequence of active Attribute Thresholds will appear in the same order as their corresponding Attribute Values.

Table 184   Device Attribute Thresholds Data Structure

Description	Bytes	Offset	Value
Data Structure Revision Number	2	00h	0010h
1st Attribute Threshold	12	02h	
…	..		
…	..		
30th Attribute Threshold	12	15Eh	
Reserved	18	16Ah	00h
Vendor specific	131	17Ch	00h
Data structure checksum	1	1FFh	
	512		

11.39.3.1   Data Structure Revision Number

This value is the same as the value used in the Device Attributes Values Data Structure.

11.39.3.2   Individual Thresholds Data Structure

The following Table defines the 12 bytes that make up the information for each Threshold entry in the Device Attribute Thresholds Data Structure. Attribute entries in the Individual Threshold Data Structure are in the same order and correspond to the entries in the Individual Attribute Data Structure.

Table 185   Individual Threshold Data Structure

Description	Bytes	Offset
Attribute ID Number (01h to FFh)	1	00h
Attribute Threshold	1	01h
Reserved (00h)	10	02h
Total Bytes	12	

11.39.3.3　Attribute ID Numbers

Attribute ID Numbers supported by the device are the same as Attribute Values Data Structures.

11.39.3.4　Attribute Threshold

These values are preset at the factory and are not meant to be changeable.

11.39.3.5　Data Structure Checksum

The Data Structure Checksum is the 2's compliment of the result of a simple 8-bit addition of the first 511 bytes in the data structure.

11.39.4　SMART Log Directory

The SMART Log Directory is SMART Log Address zero and is defined as one sector, 512 bytes, long.

Table 186　SMART Log Directory

Description	Bytes	Offset
SMART Logging Version	2	00h
Number of sectors in the log at log address 1	1	02h
Reserved	1	03h
Number of sectors in the log at log address 2	1	04h
Reserved	1	05h
…	…	…
Number of sectors in the log at log address 255	1	1Feh
Reserved	1	1FFh
	512	

The value of the SMART Logging Version word shall be 01h. The logs at log addresses 80-9Fh shall each be defined as 16 sectors long.

11.39.5　SMART Summary Error Log Sector

The following defines the 512 bytes that make up the SMART summary error log sector. All multi-byte fields shown in this data structure follow the ATA/ATAPI-7 specifications for byte ordering.

Table 187　SMART summary error log sector

Description	Bytes	Offset
SMART error log version	1	00h
Error log index	1	01h
1st error log data structure	90	02h
2nd error log data structure	90	5Ch
3rd error log data structure	90	B6h
4th error log data structure	90	110h
5th error log data structure	90	16Ah
Device error count	2	1C4h
Reserved	57	1C6h
Data structure checksum	1	1FFh
	512	

11.39.5.1　SMART Error Log Version

This value is set to 01h.

11.39.5.2　Error Log Index

This points the most recent error log data structure. Only values 1 through 5 are valid.

11.39.5.3　Device Error Count

This field contains the total number of errors. The value will not roll over.

11.39.5.4   Error Log Data Structure

Data format of each error log structure is shown below.

Table 188   Error log data structure

Description	Bytes	Offset
1st error log data structure	12	00h
2nd error log data structure	12	0Ch
3rd error log data structure	12	18h
4th error log data structure	12	24h
5th error log data structure	12	30h
Error data structure	30	3Ch
	90	

Command data structure: Data format of each command data structure is shown below.

Table 189   Command data structure

Description	Bytes	Offset
Device Control register	1	00h
Features register	1	01h
Sector count register	1	02h
Sector number register	1	03h
Cylinder Low register	1	04h
Cylinder High register	1	05h
Device/Head register	1	06h
Command register	1	07h
Timestamp (milliseconds from Power On)	4	08h
	12	

Error data structure: Data format of error data structure is shown below.

Table 190   Error data structure

Description	Bytes	Offset
Reserved	1	00h
Error register	1	01h
Sector count register	1	02h
Sector number register	1	03h
Cylinder Low register	1	04h
Cylinder High register	1	05h
Device/Head register	1	06h
Status register	1	07h
Extended error data (vendor specific)	19	08h
State	1	1Bh
Life timestamp (hours)	2	1Ch
	30	

State field contains a value indicating the device state when command was issued to the device.

Value	State
x0h	Unknown
x1h	Sleep
x2h	Standby (If the EPC feature set is enabled, Standby is standby_y or standby_z)
x3h	Active/Idle
	(If the EPC feature set is enabled, Active/Idle is idle_a or idle_b or idle_c)
x4h	SMART Off-line or Self-test
x5h-xAh	Reserved
xBh-xFh	Vendor specific
	Note**:** The value of x is vendor specific.

11.39.6   Self-Test Log Data Structure

The following defines the 512 bytes that make up the Self-test log sector. All multi-byte fields shown in these data structures follow the ATA/ATAPI-7 specifications for byte ordering.

Table 191   Self-test log data structure

Description	Bytes	Offset
Data structure revision	2	00h
Self-test number	1	n*18h+02h
Self-test execution status	1	n*18h+03h
Life time power on hours	2	n*18h+04h
Self-test failure check point	1	n*18h+06h
LBA of first failure	4	n*18h+07h
Vendor specific	15	n*18h+0Bh
…		
Vendor specific	2	1Fah
Self-test index	1	1FCh
Reserved	2	1FDh
Data structure checksum	1	1FFh
	512	

Note: n = 0 through 20

The data structure contains the descriptor of Self-test that the device has performed. Each descriptor is 24 bytes long and the self-test data structure is capable to contain up to 21 descriptors.

After 21 descriptors have been recorded, the oldest descriptor will be overwritten with new descriptor.

Self-test index points the most recent descriptor. When there is no descriptor the value is 0. When there is descriptor(s) the value is 1 through 21.

11.39.7   Selective Self-Test Log Data Structure

The Selective self-test log is a log that may be both written and read by the host. This log allows the host to select the parameters for the self-test and to monitor the progress of the self-test. The following table defines the contents of the Selective self-test log which is 512 bytes long. All multi-byte fields shown in these data structures follow the ATA/ATAPI-7 specifications for byte ordering.

Table 192   Selective self-test log data structure

Description	Bytes	Offset	Read/Write
Data structure revision	2	00h	R/W
Starting LBA for test span 1	8	02h	R/W
Ending LBA for test span 1	8	0Ah	R/W
Starting LBA for test span 2	8	12h	R/W
Ending LBA for test span 2	8	1Ah	R/W
Starting LBA for test span 3	8	22h	R/W
Ending LBA for test span 3	8	2Ah	R/W
Starting LBA for test span 4	8	32h	R/W
Ending LBA for test span 4	8	3Ah	R/W
Starting LBA for test span 5	8	42h	R/W
Ending LBA for test span 5	8	4Ah	R/W
Reserved	256	52h	Reserved
Vendor specific	154	152h	Vendor specific
Current LBA under test	8	1Ech	Read
Current span under test	2	1F4h	Read
Feature flags	2	1F6h	R/W
Vendor specific	4	1F8h	Vendor specific
Selective self-test pending time	2	1FCh	R/W
Reserved	1	1Feh	Reserved
Data structure checksum	1	1FFh	R/W
	512		

11.39.7.1   Feature Flags

The Feature flags define the features of Selective self-test to be executed.

Table 193   Selective self-test feature flags

Bit	Description
0	Vendor specific
1	When set to one, perform off-line scan after selective test.
2	Vendor specific
3	When set to one, off-line scan after selective test is pending.
4	When set to one, off-line scan after selective test is active.
5-15	Reserved.

11.39.8   Error Reporting

The following Table shows the values returned in the Status and Error Registers when specific error conditions are encountered by a device.

Table 194   SMART Error Codes

Error Condition	Status Register	Error Register
A SMART FUNCTION SET command was received by the device without the required key being loaded into the Cylinder High and Cylinder Low registers.	51h	04h
A SMART FUNCTION SET command was received by the device with a subcommand value in the Features Register that is either invalid or not supported by this device.	51h	04h
A SMART FUNCTION SET command subcommand other than SMART ENABLE OPERATIONS was received by the device while the device was in a "SMART disabled" state.	51h	04h
The device is unable to read its Attribute Values or Attribute Thresholds data structure.	51h	10h or 40h
The device is unable to write to its Attribute Values data structure.	51h	10h

11.40   Standby (E2h/96h)

The Standby command causes the device to enter the Standby Mode immediately, and set auto power down timeout parameter (standby timer).

When the Standby mode is entered, the drive is spun down but the interface remains active. If the drive is already spun down, the spin down sequence is not executed.

During the Standby mode the device will respond to commands, but there is a delay while waiting for the spindle to reach operating speed.

The automatic power down sequence is enabled and the timer starts counting down when the drive returns to Idle mode.

If the EPC feature set is enabled, device enters into the Standby_Z power condition.

Table 195   Standby Command (E2h/96h)

Command Block Output Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	0	0	0	1	0

Command Block Input Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below…							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Output Parameters To The Device

Sector Count   Timeout Parameter. If zero, the timeout interval (Standby Timer) is NOT disabled. If non-zero, then the automatic power down sequence is enabled, and the timeout interval is shown blow:

Value	Description
0	Timer disabled
1-240	Value * 5 seconds
241-251	(Value-240) * 30 minutes
252	21 minutes
253	8 hours
254	Aborted
255	21 minutes 15 seconds

When the automatic power down sequence is enabled, the drive will enter Standby mode automatically if the timeout interval expires with no drive access from the host. The timeout interval will be reinitialized if there is a drive access before the timeout interval expires.

11.41   Standby Immediate (E0h/94h)

The Standby Immediate command causes the device to enter Standby mode immediately.

The device is spun down but the interface remains active. If the device is already spun down, the spin down sequence is not executed.

During the Standby mode, the device will respond to commands, but there is a delay while waiting for the spindle to reach operating speed.

The Standby Immediate command will not affect the auto power down timeout parameter.

If the EPC feature set is enabled, device enters into the Standby_Z power condition.

Table 196   Standby Immediate Command (E0h/94h)

Command Block Output Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	0	0	0	0	0

Command Block Input Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below…							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

11.42 Write Buffer (E8h)

The Write Buffer command transfers a sector of data from the host to the sector buffer of the device. The sectors of data are transferred through the Data Register 16 bits at a time.

The Read Buffer and Write Buffer commands are synchronized such that sequential Write Buffer and Read Buffer commands access the same 512 byte within the buffer.

Table 197 Write Buffer Command (E8h)

Command Block Output Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	0	1	0	0	0

Command Block Input Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below…							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

Normal Outputs

See Normal Outputs in *Section 11.5 "Flush Cache (E7h)"*

Error Outputs

See Error Outputs in *Section 11.2 "Download Microcode (92h)"*

11.43 Write Buffer DMA (EBh)

The Write Buffer DMA command transfers a sector of data from the host to the sector buffer of the device. The sectors of data are transferred through the Data Register 16 bits at a time.

The Read Buffer and Write Buffer commands are synchronized such that sequential Write Buffer and Read Buffer commands access the same 512 byte within the buffer.

Table 198   Write Buffer DMA Command (EBh)

Command Block Output Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	0	1	0	1	1

Command Block Input Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below…							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

Normal Outputs

See Normal Outputs in *Section 11.5 "Flush Cache (E7h)"*

Error Outputs

See Error Outputs in *Section 11.2 "Download Microcode (92h)"*

11.44   Write DMA (CAh/CBh)

The Write DMA command transfers one or more sectors of data from the host to the device, then the data is written to the disk media.

The sectors of data are transferred through the Data Register 16 bits at a time.

The host initializes a slave-DMA channel prior to issuing the command. Data transfers are qualified by DMARQ and are performed by the slave-DMA channel. The device issues only one interrupt per command to indicate that data transfer has terminated and status is available.

If an uncorrectable error occurs, the write will be terminated at the failing sector.

Table 199   Write DMA Command (CAh/CBh)

Command Block Output Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	1	L	1	D	H	H	H	H
Command	1	1	0	0	1	0	1	R

Command Block Input Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below…							
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	-	-	-	-	H	H	H	H
Status	…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
V	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Output Parameters To The Device

Sector Count	The number of continuous sectors to be transferred. If zero is specified, then 256 sectors will be transferred.
Sector Number	The sector number of the first sector to be transferred. (L=0) In LBA mode, this register contains LBA bits 0 – 7. (L=1)
Cylinder High/Low	The cylinder number of the first sector to be transferred. (L=0) In LBA mode, this register contains LBA bits 8 – 15 (Low), 16 – 23 (High). (L=1)
H	The head number of the first sector to be transferred. (L=0) In LBA mode, this register contains LBA bits 24 – 27. (L=1)
R	The retry bit, but this bit is ignored.

Input Parameters From The Device

Sector Count	The number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs.
Sector Number	The sector number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 0 – 7. (L=1)
Cylinder High/Low	The cylinder number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 8 – 15 (Low), 16 – 23 (High). (L=1)
H	The head number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 24 – 27. (L=1)

11.45   Write DMA FUA Ext (3Dh)

The Write DMA FUA Ext command transfers one or more sectors of data from the host to the device, and then the data is written to the disk media.   This command provides the same function as the Write DMA Ext command except that the transferred data shall be written to the media before the ending status for this command is reported also when write caching is enabled.

The sectors of data are transferred through the Data Register 16 bits at a time.

The host initializes a slave-DMA channel prior to issuing the command. Data transfers are qualified by DMARQ and are performed by the slave-DMA channel. The device issues only one interrupt per command to indicate that data transfer has terminated and status is available.

If an unrecoverable error occurs, the write will be terminated at the failing sector.

Table 200   Write DMA FUA Ext Command (3Dh)

Command Block Output Registers		7	6	5	4	3	2	1	0
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Feature	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Sector Count	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Sector Number	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder Low	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder High	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Device/Head		-	1	-	D	-	-	-	-
Command		0	0	1	1	1	1	0	1

Command Block Input Registers		7	6	5	4	3	2	1	0
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Error		…See Below…							
Sector Count	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Sector Number	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Cylinder Low	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Cylinder High	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Device/Head		-	-	-	-	-	-	-	-
Status		…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
V	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Output Parameters To The Device

Sector Count Current	The number of continuous sectors to be transferred low order, bits (7:0).
Sector Count Previous	The number of continuous sectors to be transferred high order bits (15:8). If zero is specified in the Sector Count register, then 65,536 sectors will be transferred.
Sector Number Current	LBA (7:0).
Sector Number Previous	LBA (31:24).
Cylinder Low Current	LBA (15:8).
Cylinder Low Previous	LBA (39:32).
Cylinder High Current	LBA (23:16).

Cylinder High Previous   LBA (47:40).
Input Parameters From The Device

Sector Number (HOB=0)	LBA (7:0) of the address of the first unrecoverable error.
Sector Number (HOB=1)	LBA (31:24) of the address of the first unrecoverable error.
Cylinder Low (HOB=0)	LBA (15:8) of the address of the first unrecoverable error.
Cylinder Low (HOB=1)	LBA (39:32) of the address of the first unrecoverable error.
Cylinder High (HOB=0)	LBA (23:16) of the address of the first unrecoverable error.
Cylinder High (HOB=1)	LBA (47:40) of the address of the first unrecoverable error.

11.46 Write DMA Ext (35h)

The Write DMA Ext command transfers one or more sectors of data from the host to the device, and then the data is written to the disk media.

The sectors of data are transferred through the Data Register 16 bits at a time.

The host initializes a slave-DMA channel prior to issuing the command. Data transfers are qualified by DMARQ and are performed by the slave-DMA channel. The device issues only one interrupt per command to indicate that data transfer has terminated and status is available.

If an uncorrectable error occurs, the write will be terminated at the failing sector.

Table 201   Write DMA Ext Command (35h)

Command Block Output Registers		7	6	5	4	3	2	1	0
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Feature	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Sector Count	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Sector Number	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder Low	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder High	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Device/Head		-	1	-	D	-	-	-	-
Command		0	0	1	1	0	1	0	1

Command Block Input Registers		7	6	5	4	3	2	1	0
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Error		…See Below…							
Sector Count	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Sector Number	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Cylinder Low	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Cylinder High	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Device/Head		-	-	-	-	-	-	-	-
Status		…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
V	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Output Parameters To The Device

Sector Count Current	The number of continuous sectors to be transferred low order, bits (7:0).
Sector Count Previous	The number of continuous sectors to be transferred high order bits (15:8). If zero is specified in the Sector Count register, then 65,536 sectors will be transferred.
Sector Number Current	LBA (7:0).
Sector Number Previous	LBA (31:24).
Cylinder Low Current	LBA (15:8).
Cylinder Low Previous	LBA (39:32).
Cylinder High Current	LBA (23:16).
Cylinder High Previous	LBA (47:40).

Input Parameters From The Device

Sector Number (HOB=0) LBA (7:0) of the address of the first unrecoverable error.

Sector Number (HOB=1) LBA (31:24) of the address of the first unrecoverable error.

Cylinder Low (HOB=0) LBA (15:8) of the address of the first unrecoverable error.

Cylinder Low (HOB=1) LBA (39:32) of the address of the first unrecoverable error.

Cylinder High (HOB=0) LBA (23:16) of the address of the first unrecoverable error.

Cylinder High (HOB=1) LBA (47:40) of the address of the first unrecoverable error.

11.47 Write FPDMA Queued (61h)

The Write FPDMA Queued command transfers one or more sectors of data from the host to the device, and then the data is written to the disk media.

If an unrecoverable error occurs, the write will be terminated at the failing sector

Table 202 Write FPDMA Queued Command (61h)

Command Block Output Registers		7	6	5	4	3	2	1	0
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Feature	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Sector Count	Current	V	V	V	V	V	-	-	-
	Previous	-	-	-	-	-	-	-	-
Sector Number	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder Low	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder High	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Device/Head		V	1	-	0	-	-	-	-
Command		0	1	1	0	0	0	0	1

Command Block Input Registers		7	6	5	4	3	2	1	0
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Error		…See Below…							
Sector Count	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Sector Number	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Cylinder Low	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Cylinder High	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Device/Head		-	-	-	-	-	-	-	-
Status		…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
V	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Output Parameters To The Device

Feature Current The number of sectors to be transferred low order, bits (7:0).

Feature Previous The number of sectors to be transferred high order, bits (15:8).

Sector Count Current .

   TAG (bits 7-3) The TAG value shall be assigned to be different from all other queued commands. The value shall not exceed the maximum queue depth specified by the Word 75 of the Identify Device information.

Sector Count Previous

   PRIO (bits 7-6) The Priority (PRIO) value shall be assigned by the host based on the priority of the command issued. The device makes a best effort to complete High priority requests in a more timely fashion than Normal and isochronous priority requests. The device tries to complete isochronous requests prior to its associated deadline. The Priority values are defined as follows:

     00b   Normal priority

     01b   Isochronous – deadline dependent priority

     10b   High priority

Sector Number Current LBA (7:0)

Sector Number Previous LBA (31:24)

Cylinder Low Current LBA (15:8)

Cylinder Low Previous	LBA (39:32)
Cylinder High Current	LBA (23:16)
Cylinder High Previous	LBA (47:40)
ICC	The Isochronous Command Completion (ICC) field is valid when PRIO is set to a value of 01b. It is assigned by the host based on the intended deadline associated with the command issued. When a deadline has expired, the device continues to complete the command as soon as possible. The host can modify this behavior if the device supports the NCQ NON-DATA command (see 11.15 NCQ NON-DATA (63h)) and supports the Deadline Handling subcommand (see 11.15.2 Deadline handling Subcommand (1h)). This subcommand allows the host to set whether the device aborts commands that have exceeded the time set in ICC.

There are several parameters encoded in the ICC field: Fine or Coarse timing, Interval and the Max Time. The Interval indicates the time units of the Time Limit parameter.

If ICC Bit 7 cleared to zero, then the time interval is fine-grained.

Interval = 10msec

Time Limit = (ICC[6:0] + 1) * 10 msec

If ICC Bit 7 is set to one (coarse encoding), then the time interval is coarse grained.

Interval = 0.5 sec

Time Limit = (ICC[6:0] + 1) * 0.5 sec

Device/Head

FUA (bit 7)	When the FUA bit is set to 1, the completion status is indicated after the transferred data are written to the media also when Write Cache is enabled.
	When the FUA bit is set to 0, the completion status may be indicated before the transferred data are written to the media successfully when Write Cache is enabled.

Input Parameters From The Device

Sector Number (HOB=0)	LBA (7:0) of the address of the first unrecoverable error.
Sector Number (HOB=1)	LBA (31:24) of the address of the first unrecoverable error.
Cylinder Low (HOB=0)	LBA (15:8) of the address of the first unrecoverable error.
Cylinder Low (HOB=1)	LBA (39:32) of the address of the first unrecoverable error.
Cylinder High (HOB=0)	LBA (23:16) of the address of the first unrecoverable error.
Cylinder High (HOB=1)	LBA (47:40) of the address of the first unrecoverable error.

11.48 Write Log Ext (3Fh)

This command writes a specified number of 512 byte data sectors to the specific log. The device shall interrupt for each DRQ block transferred.

Table 203 Write Log Ext Command (3Fh

Command Block Output Registers		7	6	5	4	3	2	1	0
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Feature	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Sector Count	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Sector Number	Current	V	V	V	V	V	V	V	V
	Previous	-	-	-	-	-	-	-	-
Cylinder Low	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder High	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Device/Head		1	-	1	D	-	-	-	-
Command		0	0	1	1	1	1	1	1

Command Block Input Registers		7	6	5	4	3	2	1	0
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Error		…See Below…							
Sector Count	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Sector Number	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Cylinder Low	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Cylinder High	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Device/Head		-	-	-	-	-	-	-	-
Status		…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	V	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Output Parameters To The Device

Sector Count Current — The number of sectors to be written to the specified log low order, bits (7:0).

Sector Count Previous — The number of sectors to be written to the specified log high orders, bits (15:8). If the number of sectors is greater than the number indicated in the Log directory, which is available in Log number zero, the device shall return command aborted. The log transferred to the device shall be stored by the device starting at the first sector in the specified log.

Sector Number Current — The log to be written as described in Table 140 Log address definition. If the host attempts to write to a read only log address, the device shall return command aborted.

Cylinder Low Current — The first sector of the log to be written low order, bits (7:0).

Cylinder Low Previous — The first sector of the log to be written high order, bits (15:8).

If the feature set associated with the log specified in the Sector Number register is not supported or enabled, or if the values in the Sector Count, Sector Number or Cylinder Low registers are invalid, the device shall return command aborted. If the host attempts to write to a read only log address, the device shall return command aborted.

11.49   Write Log DMA Ext (57h)

The content of this command is the same as Write Log Ext. See previous *Section 11.52 "Write Log Ext (3Fh)"*.

Table 204   Write Log DMA Ext Command (57h)

Command Block Output Registers		7	6	5	4	3	2	1	0
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Feature	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Sector Count	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
LBA Low	Current	V	V	V	V	V	V	V	V
	Previous	-	-	-	-	-	-	-	-
LBA Mid	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
LBA High	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Device		-	-	-	-	-	-	-	-
Command		0	1	0	1	0	1	1	1

Command Block Input Registers		7	6	5	4	3	2	1	0
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Error				...See Below...					
Sector Count	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
LBA Low	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
LBA Mid	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
LBA High	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Device		-	-	-	-	-	-	-	-
Status				...See Below...					

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
V	V	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	0	V

11.50   Write Multiple (C5h)

The Write Multiple command transfers one or more sectors from the host to the device, and then the data is written to the disk media.

Command execution is identical to the Write Sector(s) command except that an interrupt is generated for each block (as defined by the Set Multiple command) instead of for each sector. The sectors are transferred through the Data Register 16 bits at a time.

Table 205   Write Multiple Command (C5h)

Command Block Output Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	1	L	1	D	H	H	H	H
Command	1	1	0	0	0	1	0	1

Command Block Input Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	-	-	-	-	H	H	H	H
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Output Parameters To The Device

Sector Count	The number of continuous sectors to be transferred. If zero is specified, then 256 sectors will be transferred.
Sector Number	The sector number of the first sector to be transferred. (L=0) In LBA mode, this register contains LBA bits 0 - 7. (L=1)
Cylinder High/Low	The cylinder number of the first sector to be transferred. (L=0) In LBA mode, this register contains LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
H	The head number of the first sector to be transferred. (L=0) In LBA mode, this register contains LBA bits 24 - 27. (L=1)

Input Parameters From The Device

Sector Count	The number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs.
Sector Number	The sector number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 0 - 7. (L=1)
Cylinder High/Low	The cylinder number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
H	The head number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 24 - 27. (L=1)

11.51 Write Multiple Ext (39h)

The Write Multiple Ext command transfers one or more sectors from the host to the device, and then the data is written to the disk media.

Command execution is identical to the Write Sector(s) Ext command except that an interrupt is generated for each block (as defined by the Set Multiple command) instead of for each sector. The sectors are transferred through the Data Register 16 bits at a time.

Table 206 Write Multiple Ext Command (39h)

Command Block Output Registers		7	6	5	4	3	2	1	0
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Feature	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Sector Count	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Sector Number	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder Low	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder High	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Device/Head		-	1	-	D	-	-	-	-
Command		0	0	1	1	1	0	0	1

Command Block Input Registers		7	6	5	4	3	2	1	0
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Error				...See Below...					
Sector Count	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Sector Number	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Cylinder Low	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Cylinder High	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Device/Head		-	-	-	-	-	-	-	-
Status				...See Below...					

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Output Parameters To The Device

Sector Count Current	The number of continuous sectors to be transferred low order, bits (7:0)
Sector Count Previous	The number of continuous sectors to be transferred high order, bits (15:8). If zero is specified in the Sector Count register, then 65,536 sectors shall be transferred.
Sector Number Current	LBA (7:0).
Sector Number Previous	LBA (31:24).
Cylinder Low Current	LBA (15:8).
Cylinder Low Previous	LBA (39:32).
Cylinder High Current	LBA (23:16).
Cylinder High Previous	LBA (47:40).

Input Parameters From The Device

Sector Number (HOB=0)	LBA (7:0) of the address of the first unrecoverable error.
Sector Number (HOB=1)	LBA (31:24) of the address of the first unrecoverable error.
Cylinder Low (HOB=0)	LBA (15:8) of the address of the first unrecoverable error.
Cylinder Low (HOB=1)	LBA (39:32) of the address of the first unrecoverable error.
Cylinder High (HOB=0)	LBA (23:16) of the address of the first unrecoverable error.
Cylinder High (HOB=1)	LBA (47:40) of the address of the first unrecoverable error.

11.52   Write Multiple FUA Ext (CEh)

The Write Multiple Ext command transfers one or more sectors from the host to the device, and then the data is written to the disk media.   This command provides the same function as the Write Multiple Ext command except that the transferred data shall be written to the media before the ending status for this command is reported also when write caching is enabled.

Command execution is identical to the Write Sector(s) Ext command except that an interrupt is generated for each block (as defined by the Set Multiple command) instead of for each sector. The sectors are transferred through the Data Register 16 bits at a time.

Table 207   Write Multiple FUA Ext Command (CEh)

Command Block Output Registers		7	6	5	4	3	2	1	0
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Feature	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Sector Count	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Sector Number	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder Low	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder High	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Device/Head		-	1	-	D	-	-	-	-
Command		1	1	0	0	1	1	1	0

Command Block Input Registers		7	6	5	4	3	2	1	0
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Error					...See Below...				
Sector Count	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Sector Number	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Cylinder Low	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Cylinder High	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Device/Head		-	-	-	-	-	-	-	-
Status					...See Below...				

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Output Parameters To The Device

Sector Count Current   The number of continuous sectors to be transferred low order, bits (7:0)

Sector Count Previous   The number of continuous sectors to be transferred high order, bits (15:8).   If zero is specified in the Sector Count register, then 65,536 sectors shall be transferred.

Sector Number Current   LBA (7:0).

Sector Number Previous   LBA (31:24).

Cylinder Low Current   LBA (15:8).

Cylinder Low Previous   LBA (39:32).

Cylinder High Current   LBA (23:16).

Cylinder High Previous   LBA (47:40).

Input Parameters From The Device

Sector Number (HOB=0)   LBA (7:0) of the address of the first unrecoverable error.

Sector Number (HOB=1)   LBA (31:24) of the address of the first unrecoverable error.

Cylinder Low (HOB=0)   LBA (15:8) of the address of the first unrecoverable error.

Cylinder Low (HOB=1)   LBA (39:32) of the address of the first unrecoverable error.

Cylinder High (HOB=0)   LBA (23:16) of the address of the first unrecoverable error.

Cylinder High (HOB=1)   LBA (47:40) of the address of the first unrecoverable error.

11.53   Write Sector(s) (30h/31h)

The Write Sector(s) command transfers one or more sectors from the host to the device, and then the data is written to the disk media.

The sectors are transferred through the Data Register 16 bits at a time.

If an uncorrectable error occurs, the write will be terminated at the failing sector.

Table 208   Write Sector(s) Command (30h/31h)

Command Block Output Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	1	L	1	D	H	H	H	H
Command	0	0	1	1	0	0	0	R

Command Block Input Registers	7	6	5	4	3	2	1	0
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	-	-	-	-	H	H	H	H
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

utput Parameters To The Device

Sector Count	The number of continuous sectors to be transferred. If zero is specified, then 256 sectors will be transferred.
Sector Number	The sector number of the first sector to be transferred. (L=0) In LBA mode, this register contains LBA bits 0 - 7. (L=1)
Cylinder High/Low	The cylinder number of the first sector to be transferred. (L=0) In LBA mode, this register contains LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
H	The head number of the first sector to be transferred. (L=0) In LBA mode, this register contains LBA bits 24 - 27. (L=1)
R	The retry bit, but this bit is ignored.

Input Parameters From The Device

Sector Count	The number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs.
Sector Number	The sector number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 0 - 7. (L=1)
Cylinder High/Low	The cylinder number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
H	The head number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 24 - 27. (L=1)

11.54 Write Sector(s) Ext (34h)

The Write Sector(s) Ext command transfers one or more sectors from the host to the device, and then the data is written to the disk media.

The sectors are transferred through the Data Register 16 bits at a time.

If an uncorrectable error occurs, the write will be terminated at the failing sector.

Table 209   Write Sector(s) Ext Command (34h)

Command Block Output Registers		7	6	5	4	3	2	1	0
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Feature	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Sector Count	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Sector Number	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder Low	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder High	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Device/Head		-	1	-	D	-	-	-	-
Command		0	0	1	1	0	1	0	0

Command Block Input Registers		7	6	5	4	3	2	1	0
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Error		...See Below...							
Sector Count	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Sector Number	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Cylinder Low	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Cylinder High	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Device/Head		-	-	-	-	-	-	-	-
Status		...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Output Parameters To The Device

Sector Count Current	The number of continuous sectors to be transferred low order, bits (7:0).
Sector Count Previous	The number of continuous sectors to be transferred high order bits (15:8). If zero is specified, then 65,536 sectors will be transferred.
Sector Number Current	LBA (7:0).
Sector Number Previous	LBA (31:24).
Cylinder Low Current	LBA (15:8).
Cylinder Low Previous	LBA (39:32).
Cylinder High Current	LBA (23:16).
Cylinder High Previous	LBA (47:40).

Input Parameters From The Device

Sector Number (HOB=0)	LBA (7:0) of the address of the first unrecoverable error.
Sector Number (HOB=1)	LBA (31:24) of the address of the first unrecoverable error.
Cylinder Low (HOB=0)	LBA (15:8) of the address of the first unrecoverable error.
Cylinder Low (HOB=1)	LBA (39:32) of the address of the first unrecoverable error.
Cylinder High (HOB=0)	LBA (23:16) of the address of the first unrecoverable error.
Cylinder High (HOB=1)	LBA (47:40) of the address of the first unrecoverable error.

11.55   Write Stream Ext (3Bh)

This command writes from 1 to 65536 sectors as specified in the Sector Count register.   A sector count of 0 requests 65536 sectors.

If the Write Continuous bit is set to one, the device shall not stop execution of the command due to errors.   If the WC bit is set to one and errors occur in the transfer or writing of the data, the device shall continue to transfer the amount of data requested and then provide ending status with the BSY bit cleared to zero, the SE bit set to one, the ERR bit cleared to zero, and the type of error, IDNF, or ABRT, reported in the error log.   If the WC bit is set to one and the Command Completion Time Limit expires, the device shall stop execution of the command and provide ending status with BSY bit cleared to zero, the SE bit set to one, the ERR bit cleared to zero, and report the fact that the Command Completion Time Limit expired by setting the CCTO bit in the error log to one,   In all cases, the device shall attempt to transfer the amount of data requested within the Command Completion Time Limit event if some data transferred is in error.

Table 210   Write Stream Ext Command (3Bh)

Command Block Output Registers		7	6	5	4	3	2	1	0
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Feature	Current	V	V	V	V	-	V	V	V
	Previous	V	V	V	V	V	V	V	V
Sector Count	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Sector Number	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder Low	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder High	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Device/Head		1	1	1	D	-	-	-	-
Command		0	0	1	1	1	0	1	1

Command Block Input Registers		7	6	5	4	3	2	1	0
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Error		...See Below...							
Sector Count	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Sector Number	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Cylinder Low	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Cylinder High	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Device/Head		-	-	-	-	-	-	-	-
Status		...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	CCTO
V	0	0	V	0	V	0	V

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	SE	DWE	DRQ	COR	IDX	ERR
0	V	V	0	-	0	-	V

Output Parameters To The Device

Feature Current

URG (bit7)   URG specifies an urgent transfer request.   The Urgent bit specifies that the command should be completed in the minimum possible time by the device and shall be completed within the specified Command Completion Time Limit.

WC   (bit6)   WC specifies Write Continuous mode enabled.   If the Write Continuous bit is set to one, the device shall not stop execution of the command due to errors.

If the WC bit is set to one and errors occur in transfer or writing of the data, the device shall continue to transfer the amount of data requested and then provide ending status with BSY bit cleared to zero, the SE bit set to one, the ERR bit cleared to zero, and the type of error, IDNF or ABRT reported in the error log.

If the WC bit is set to one and the Command Completion Time Limit expires, the device shall stop execution of the command and provide ending status with the BSY bit cleared to zero, the SE bit set to one, the ERR bit cleared to zero, and report the fact that the Command Completion Time Limit expired by setting the CCTO bit in the error log to one.

In all cases, the device shall attempt to transfer the amount of data requested within the Command Completion Time Limit even if some data transferred is in error.

F (bit5)   F specifies that all data for the specified stream shall be flushed to the media before command complete is reported when set to one.

HSE (bit4)   HSE (Handle Stream Error) specifies that this command starts at the LBA of the last reported error for this stream, so the device may attempt to continue its corresponding error recovery sequence where it left off earlier.

Stream ID (bit 0..2)   Stream ID specifies the stream being written.   The device shall operate according to the Stream ID set by the Write Stream command.

Feature Previous   The time allowed for the current command's completion is calculated as follows:

Command Completion Time Limit = (content of the Feature register Previous) * (Identify Device words (99:98)) u seconds

If the value is zero, the device shall use the Default CCTL supplied with a previous Configure Stream command for this Stream ID.   If the Default CCTL is zero, or no previous Configure Stream command was defined for this Stream ID, the device will ignore the CCTL.   The time is measured from the write of the command register to the final INTRQ for command completion. The device has minimum CCTL value. When the specified value is shorter than the minimum value, CCTL is set to the minimum value. Actual minimum CCTL value is described in the "Deviations from Standard" section.

Sector Count Current   The number of continuous sectors to be transferred low order, bits (7:0)

Sector Count Previous   The number of continuous sectors to be transferred high order, bits (15:8).   If zero is specified in the Sector Count register, then 65,536 sectors will be transferred.

Sector Number Current   LBA (7:0).

Sector Number Previous   LBA (31:24).

Cylinder Low Current   LBA (15:8).

Cylinder Low Previous   LBA (39:32).

Cylinder High Current   LBA (23:16).

Cylinder High Previous   LBA (47:40).

Input Parameters From The Device

Sector Number (HOB=0)	LBA (7:0) of the address of the first unrecoverable error.
Sector Number (HOB=1)	LBA (31:24) of the address of the first unrecoverable error.
Cylinder Low (HOB=0)	LBA (15:8) of the address of the first unrecoverable error.
Cylinder Low (HOB=1)	LBA (39:32) of the address of the first unrecoverable error.
Cylinder High (HOB=0)	LBA (23:16) of the address of the first unrecoverable error.
Cylinder High (HOB=1)	LBA (47:40) of the address of the first unrecoverable error.
CCTO (Error, bit 0)	CCTO bit shall be set to one if a Command Completion Time Limit Out error has occurred.

11.56 Write Uncorrectable Ext (45h)

The Write Uncorrectable Ext command is used to cause the device to report an uncorrectable error when the target sector is subsequently read.

When the Feature field contains a value of 55h the Write Uncorrectable Ext command shall cause the device to indicate a failure when reads to any of the sectors that are contained in physical block of specified sector are performed. These sectors are referred to as 'pseudo uncorrectable' sectors. In this case whenever a pseudo uncorrectable sector is accessed via a read command the drive shall perform normal error recovery to the fullest extent and then set the UNC and ERR bits to indicate the sector is bad.

When the Feature field(7:0) contains a value of AAh the Write uncorrectable ext command shall cause the device to flag the specified sector as 'flagged uncorrectable'. Flagging a logical sector as uncorrectable shall cause the device to indicate a failure when reads to the specified sector are performed. These sectors are referred to as 'flagged uncorrectable' sectors. In this case whenever a 'flagged uncorrectable' sector is accessed via a read command the device shall set the UNC and ERR bits to indicate the sector is bad.

If this command is sent to the device with the content of the Features field(7:0) set to anything other than what is defined above the device shall abort the command.

Commands that return UNC and ERR when a pseudo uncorrectable or flagged uncorrectable sector is read include: READ DMA, READ DMA EXT, READ MULTIPLE, READ MULTIPLE EXT, READ SECTOR(S), READ SECTOR(S) EXT, READ VERIFY SECTOR(S), READ, VERIFY SECTOR(S) EXT, READ STREAM EXT.

EXT. if the host writes to a 'pseudo uncorrectable' or 'flagged uncorrectable' sector, the drive shall attempt to write the data to the sector. The write shall clear the uncorrectable status of the sector and make the sector good if possible and the device shall verify that the sector may now be read without error. It is possible that an 'uncorrectable' sector location has actual physical errors. In this case read commands and/or write commands shall return ERR status information that is consistent with the error. The pseudo uncorrectable or flagged uncorrectable status of a sector shall remain through a power cycle. If the drive is unable to process a Write Uncorrectable EXT command for any reason the device shall abort the command.

Table 211   Write Uncorrectable Ext Command (45h)

Command Block Output Registers		7	6	5	4	3	2	1	0
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Feature	Current	V	V	V	V	V	V	V	V
	Previous	-	-	-	-	-	-	-	-
Sector Count	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Sector Number	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder Low	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder High	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Device/Head		-	1	-	D	-	-	-	-
Command		0	1	0	0	0	1	0	1

Command Block Input Registers		7	6	5	4	3	2	1	0
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Error		...See Below...							
Sector Count	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Sector Number	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Cylinder Low	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Cylinder High	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Device/Head		-	-	-	-	-	-	-	-
Status		...See Below...							

Table continued on next page →

			Error Register									Status Register				
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	V	0	V	0	0		0	V	0	V	-	0	-	V

Output Parameters To The Device

Feature Current	Uncorrectable options
	55h :Create a pseudo-uncorrectable error with logging
	AAh :Created a flagged error without logging
	Other value : Reserved
Sector Count Current	The number of continuous sectors to be transferred low order, bits (7:0).
Sector Count Previous	The number of continuous sectors to be transferred high order bits (15:8). I zero is specified, then 65,536 sectors will be transferred.
Sector Number Current	LBA (7:0).
Sector Number Previous	LBA (31:24).
Cylinder Low Current	LBA (15:8).
Cylinder Low Previous	LBA (39:32).
Cylinder High Current	LBA (23:16).
Cylinder High Previous	LBA (47:40).

Input Parameters From The Device

Sector Number (HOB=0)	LBA (7:0) of the address of the first unrecoverable error.
Sector Number (HOB=1)	LBA (31:24) of the address of the first unrecoverable error.
Cylinder Low (HOB=0)	LBA (15:8) of the address of the first unrecoverable error.
Cylinder Low (HOB=1)	LBA (39:32) of the address of the first unrecoverable error.
Cylinder High (HOB=0)	LBA (23:16) of the address of the first unrecoverable error.
Cylinder High (HOB=1)	LBA (47:40) of the address of the first unrecoverable error.